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Design and Analysis of Hybrid GDI-PTL Based Wallace Tree Multipliers for Low-Power DCT Architecture in Image Compression

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Abstract

This paper presents a hybrid low-power Wallace Tree multiplier architecture employing Gate Diffusion Input (GDI) and Pass Transistor Logic (PTL) techniques, specifically designed for efficient integration into Discrete Cosine Transform (DCT)-based image compression systems. The proposed design incorporates a novel hybrid full adder that leverages the low-power advantages of GDI and the high-speed characteristics of PTL, resulting in a compact, power-optimized solution. GDI logic is utilized for less-transistor-count realization of sum and carry logic, while PTL enhances XOR computation and signal propagation with minimal delay and area overhead. This hybrid adder is embedded into a Wallace Tree multiplier, which serves as a critical computational block within the 2D-DCT transform engine, commonly used in JPEG image compression. The multiplier's efficient structure significantly reduces the number of logic stages needed for partial product reduction, ensuring high throughput and reduced switching activity. Implemented in 90 nm and 45 nm CMOS technologies, the design achieves notable improvements in power-delay product (PDP), area, and energy efficiency when compared to conventional CMOS or single-style logic designs. Simulation of the design is performed using Cadence EDA spectre simulator, results up to a 10× reduction in power consumption and substantial area savings. These results establish the hybrid GDI-PTL-based Wallace Tree multiplier as a highly suitable solution for real-time and portable image processing applications, including mobile devices, low-power high efficiency video encoders, and energy-constrained embedded systems.

Keywords: Hybrid full adder, GDI logic, PTL, Wallace Tree multiplier, 2D-DCT, image compression, Low power, area optimization, delay reduction

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1. Introduction

In modern digital electronics, arithmetic operations such as addition and multiplication constitute the computational foundation of systems used in image processing, signal processing, cryptography, and embedded communication platforms. With the rapid growth of multimedia and medical imaging applications, hardware accelerators must achieve high computational throughput while operating under strict constraints of silicon area, power consumption, and energy efficiency. Multipliers, being one of the most resource-intensive arithmetic blocks, significantly influence the overall performance of digital signal processing architectures. In transform-based compression techniques such as the 2D Discrete Cosine Transform (2D-DCT), multiplication with constant cosine coefficients dominates the computational complexity and power consumption. Therefore, optimization

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of multiplier architectures is essential for designing low-power and high-performance VLSI systems.

Traditional CMOS-based implementations provide reliable full-swing outputs and robust noise margins. However, they often require a large transistor count and exhibit considerable dynamic power dissipation due to high switching activity. As technology scales into deep submicron regimes, these limitations become more pronounced. To address these challenges, alternative logic design styles such as Pass Transistor Logic (PTL) and Gate Diffusion Input (GDI) have been explored for arithmetic circuit design. PTL reduces transistor count and capacitance by allowing signals to propagate through pass devices instead of complementary pull-up and pull-down networks. However, threshold voltage degradation and reduced output swing can affect performance and reliability at advanced nodes. The GDI technique offers compact logic realization with fewer transistors and reduced switching activity, enabling lower dynamic power consumption. By carefully designing arithmetic units using these alternative logic styles, improved power-delay trade-offs can be achieved. Among multiplier architectures, the Wallace Tree structure is widely adopted for high-speed multiplication due to its efficient partial product reduction mechanism using parallel compression stages. Since the performance of a Wallace Tree multiplier strongly depends on the efficiency of its underlying full and half adders, optimizing these building blocks at the circuit level becomes critical for overall system improvement. In transform-based architectures such as DCT processors for image compression standards including JPEG and MPEG, multiplier optimization directly translates into improved energy efficiency. Therefore, exploring compact and low-power arithmetic logic styles for multiplier implementation remains an important research direction in advanced VLSI design.

2. Related Work

Energy-efficient full adder design has been extensively investigated using hybrid-CMOS, PTL, and GDI logic styles. Goel et al. [3] proposed a robust hybrid-CMOS full adder optimized for deep-submicrometer technologies, emphasizing signal integrity and energy efficiency. While their design improves robustness, it relies on higher transistor counts and does not specifically target multiplier integration. The GDI logic technique introduced by Morgenshtein et al. [2] demonstrated significant transistor count reduction for combinational circuits. However, its application to high-speed arithmetic compressor stages within Wallace tree multipliers remains limited. PTL-based full adders and multipliers have been investigated by D. B. R. et al. [5] and K. B. B et al. [6], showing reduced power consumption at 90 nm technology. Despite improvements in compactness, PTL designs suffer from threshold voltage degradation and incomplete swing restoration, which may degrade performance at scaled nodes. At the architectural level, Wallace [1] introduced the fast reduction tree multiplier, and Parhami [4] later proposed low-power Wallace tree optimizations. More recent arithmetic implementations, including Wallace-based adders and ALUs in [7], [8], focus on system-level integration and architectural efficiency.

In contrast to prior works, the present study introduces a selectively hybrid GDI–PTL full adder optimized for timing-critical compressor stages within the Wallace tree structure. Unlike existing approaches that address either logic-style efficiency or architectural optimization independently, the proposed work integrates transistor-level hybridization within a high-speed multiplier framework, achieving improved delay, reduced transistor count, and enhanced scalability.

3. Methodology

Modern VLSI design relies on efficient logic families to balance speed, power, and area requirements. CMOS logic remains the most widely used technique due to its robustness and full voltage swing, but its higher transistor count often results in larger area and increased power dissipation. On the other hand, Pass Transistor Logic (PTL) achieves compact circuits with fewer transistors, making it attractive for arithmetic and combinational blocks, though it suffers from threshold voltage drop and reduced driving capability. To address these limitations, the Gate Diffusion Input (GDI) approach has been introduced, offering compact implementations like PTL while preserving signal quality closer to CMOS. This makes GDI particularly suitable for low-power and high-performance applications such as multipliers and adders.

3.1. Gate Diffusion Input (GDI) Technique for Low-Power Design

Gate Diffusion Input (GDI) is a promising digital design methodology that enables the implementation of complex logic functions with a significantly reduced transistor count compared to conventional CMOS logic. The basic GDI cell resembles an inverter but with three inputs:

- **G (Gate):** Connected to the gates of both NMOS and PMOS transistors
- **P (PMOS source):** Connected to the source/drain of the PMOS
- **N (NMOS source):** Connected to the source/drain of the NMOS
- **Output:** Taken from the common drain of the PMOS and NMOS

This proposed structure facilitates compact realization of logic functions with minimal parasitic capacitance and switching activity. In arithmetic circuits such as adders and multipliers, using GDI logic significantly reduces dynamic power and propagation delay, making it ideal for low-power, high-speed VLSI systems.

3.2. Hybrid Full Adder Using GDI and PTL Techniques

To further enhance power and area efficiency, a hybrid low-power full adder combining GDI and Pass Transistor Logic (PTL) techniques has been employed. GDI excels in generating logic functions with reduced capacitance and transistor count, while PTL utilizes transistors as switches to pass signals directly, minimizing the need for complementary networks.The hybrid architecture employs GDI logic for generating intermediate signals (such as carry and propagate) and PTL for efficient XOR logic and output routing. This strategic integration exploits the strengths of both techniques lower power from GDI and faster signal transitions from PTL resulting in reduced power-delay product (PDP) and compact silicon area. The hybrid design is particularly suited for low-voltage operations, making it ideal for energy-constrained environments like mobile devices and battery-powered sensors.Simulation results confirm that the hybrid GDI-PTL full adder outperforms conventional CMOS and standalone GDI or PTL designs in terms of power consumption, delay, and area. These advantages make the hybrid approach a strong candidate for integration in complex arithmetic architectures.

3.3. Integration of Hybrid Full Adder in Wallace Tree Multiplier for 2D DCT

In the proposed architecture, the hybrid GDI-PTL full adder is embedded within the Wallace Tree multiplier, a parallel multiplier structure optimized for reducing partial product layers efficiently. This is particularly beneficial in Discrete Cosine Transform (DCT)-based image compression pipelines, where rapid and power-efficient multiplication is crucial. The Wallace Tree reduces the latency of multiplication by performing parallel additions of partial products, and the integration of the hybrid GDI-PTL full adder further accelerates this process while minimizing power. GDI logic contributes to low switching activity and reduced internal capacitance, whereas PTL ensures high-speed signal propagation. By employing GDI-based half and full adders within the Wallace Tree structure, the proposed multiplier significantly improves energy efficiency. This directly translates to enhanced performance of the 2D DCT core, which is a computational bottleneck in real-time image compression tasks. The hybrid Wallace Tree multiplier shows notable improvements in power, delay, and area metrics compared to traditional CMOS-based designs, as verified through post-synthesis simulations. The architecture is thus highly suitable for low-power image compression systems, such as mobile imaging, video encoders, and wearable biomedical applications, where energy consumption and processing speed are critical.

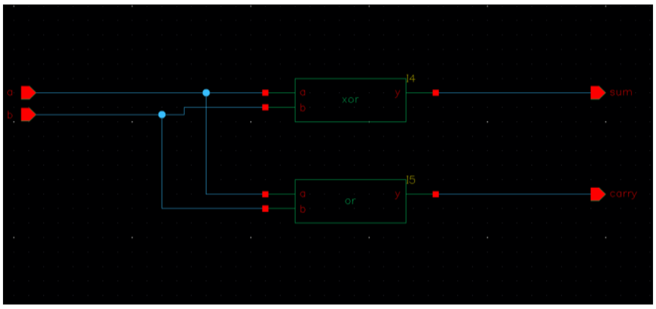

Figure 1. Schematic diagram of half adder using GDI technology

GDI based AND and XOR logic are used to design half adder. The novelty shown in the Fig 1, makes the combination to provide full swing half adder. In this proposed Full Adder, we use Hybrid GDI based AND, OR, and XOR gates. With comparison to previous work, the novelty present in the proposed work makes the circuit as low power and area reduction.

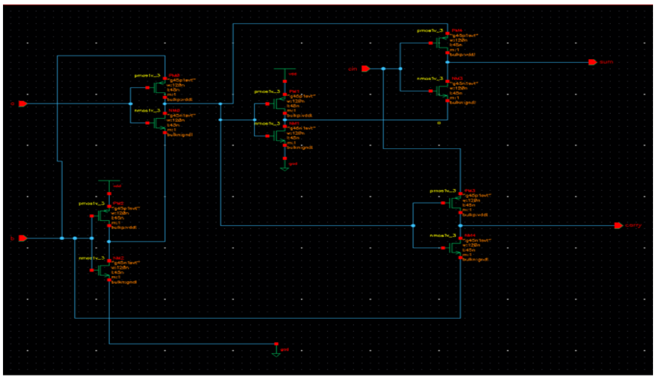

Figure 2. Schematic diagram of Full Adder Using GDI-10T

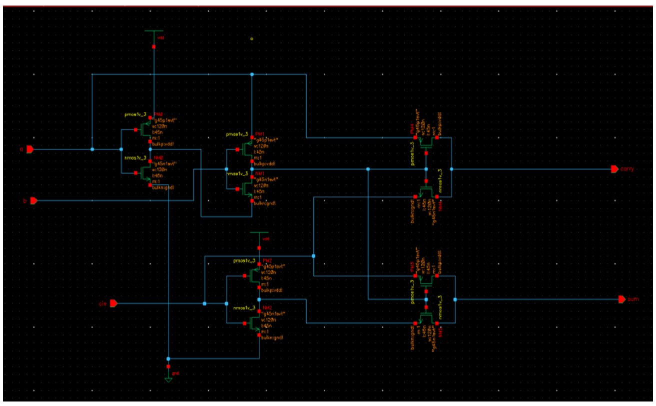

Figure 3. Schematic diagram of Full Adder using Hybrid GDI- PTL

The full adder schematic shown in Figure 3**.** demonstrates a successful implementation of a Hybrid GDI-PTL logic style using Cadence Virtuoso EDA tool. This design effectively integrates Gate Diffusion Input (GDI) logic for its low transistor count and Pass Transistor Logic (PTL) for high-speed signal propagation. The architecture efficiently computes both sum and carry outputs with a minimal number of transistors, resulting in reduced power consumption, area**,** and delay. Simulation results for this circuit show a delay of 21.3 ps**,** power consumption around 327.9 nW, and a transistor count of just 10 per full adder cell, depending on the variant used. This makes it highly suitable for scalable arithmetic units like Wallace Tree Multipliers **in** real-time, low-power applications**.** Thus, this hybrid full adder design exemplifies a practical and efficient alternative to conventional CMOS-based adders, particularly in deep submicron nodes like 45 nm where power and area constraints are critical**.**

3.4. Wallace Tree Multiplier

Efficient multiplication is a fundamental requirement in digital signal processing, particularly in transform-based image compression techniques such as the Discrete Cosine Transform (DCT) [20]. In this context, the Wallace Tree multiplier [27**]** stands out as a high-speed hardware-efficient architecture for performing parallel multiplication. Originally proposed by Chris Wallace, this structure significantly reduces the critical path delay by minimizing the number of sequential addition stages required to sum the partial products. Unlike conventional array multipliers that suffer from linear delay growth with operand size, the Wallace Tree uses a tree-like interconnection of carry-save adders and compressors to achieve logarithmic delay complexity. Due to its parallelism and reduced propagation delay, the Wallace Tree architecture is particularly suited for real-time image and video compression, where speed and power efficiency are crucial. Integrating this multiplier into DCT computation blocks allows for faster coefficient generation and improved throughput, directly impacting compression speed and energy efficiency. The performance of a Wallace Tree multiplier is highly dependent on the logic style used in its partial product reduction and adder stages. Conventional CMOS logic, although robust and noise tolerant, incurs significant delay and power penalties due to its large transistor count, high parasitic capacitances, and full rail-to-rail switching activity. Pass Transistor Logic (PTL) offers reduced transistor usage and lower switching activity; however, it suffers from threshold voltage degradation, limited driving capability, and poor signal integrity in cascaded stages, making it unsuitable for deeply pipelined or high-speed arithmetic structures. Pure Gate Diffusion Input (GDI) logic addresses these limitations by enabling complex logic functions with fewer transistors and reduced capacitance, yet it still faces challenges related to signal restoration and scalability in certain paths. To overcome these limitations, this work proposes a Hybrid GDI–PTL logic style**,** which constitutes the key novelty of the methodology. In the proposed approach, GDI cells are strategically employed in timing-critical and logic-intensive paths to ensure full-swing operation and fast signal generation, while PTL is selectively applied in non-critical paths to minimize transistor count, switching activity, and area overhead. This complementary integration effectively mitigates PTL voltage degradation through GDI-based signal reinforcement and achieves a balanced trade-off between speed, power, and area, making the hybrid logic particularly well suited for high-performance Wallace Tree multiplier architectures. Multiplier structure is presented in Fig 4. to demonstrate the usefulness of the suggested AND, half adder, and full adder. Unlike conventional Wallace implementations that focus solely on structural reduction of partial products, the proposed design introduces logic-level optimization within each reduction stage. By embedding the hybrid GDI–PTL full adder in every compression node, the multiplier benefits from both architectural parallelism and transistor-level power optimization, a combination not explicitly addressed in prior low-power Wallace tree implementations such as Parhami [4] or [7], [8] reported designs.

3.5. Novelty of the Proposed Hybrid GDI–PTL Full Adder

The novelty of the proposed hybrid GDI–PTL full adder lies in its transistor-level optimization, embedded swing restoration mechanism, and critical-path reduction strategy, which collectively distinguish it from existing hybrid-CMOS, pure PTL, and standalone GDI implementations reported in the literature. Unlike conventional hybrid-CMOS full adders such as those by Goel *et al.* [3], which rely on complementary pull-up and pull-down networks resulting in higher transistor count and switching capacitance, the proposed design eliminates redundant complementary structures through selective logic partitioning between GDI and PTL domains. The XOR/XNOR functionality is realized using compact GDI cells to minimize internal capacitance and switching activity, while carry generation is structured using optimized pass-transistor paths to shorten propagation depth. In contrast to prior PTL-based adders that suffer from threshold voltage degradation and reduced output swing, the proposed architecture incorporates GDI-based reinforcement at critical internal nodes, thereby ensuring full voltage swing without additional restoration buffers. This integrated swing stabilization approach improves signal integrity under deep-submicron conditions while preserving compactness. Furthermore, by carefully restructuring the carry propagation path, the number of cascaded pass devices is reduced, leading to a shorter critical path and improved delay performance. The resulting design achieves a reduced transistor count per full adder cell compared to most reported hybrid implementations, while simultaneously improving power-delay product. When embedded into the Wallace Tree multiplier structure, these transistor-level enhancements directly translate into lower partial-product compression latency and reduced dynamic power consumption, establishing the proposed architecture as a balanced, scalable, and energy-efficient solution for high-performance arithmetic units in 90 nm and 45 nm CMOS technologies.

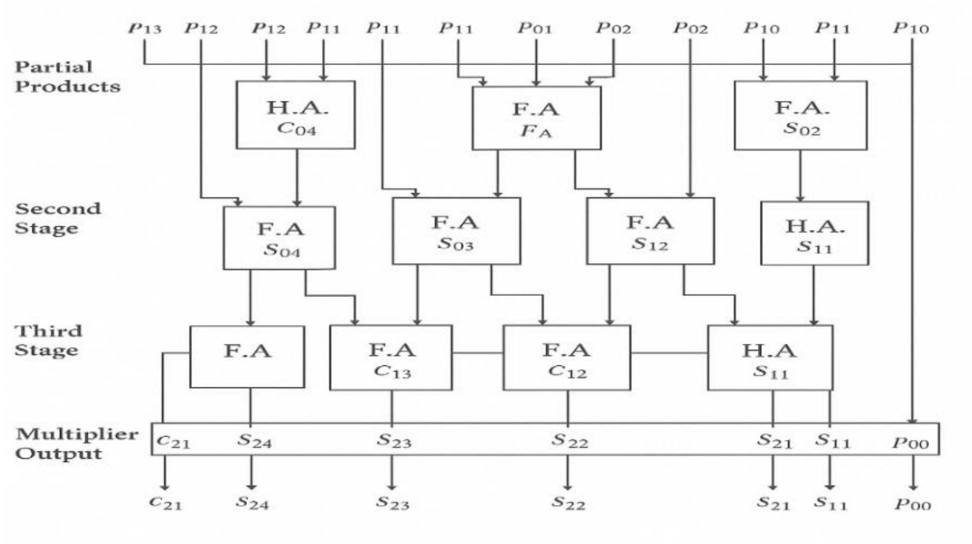

Figure 4. Schematic diagram of Wallace Tree Multiplier

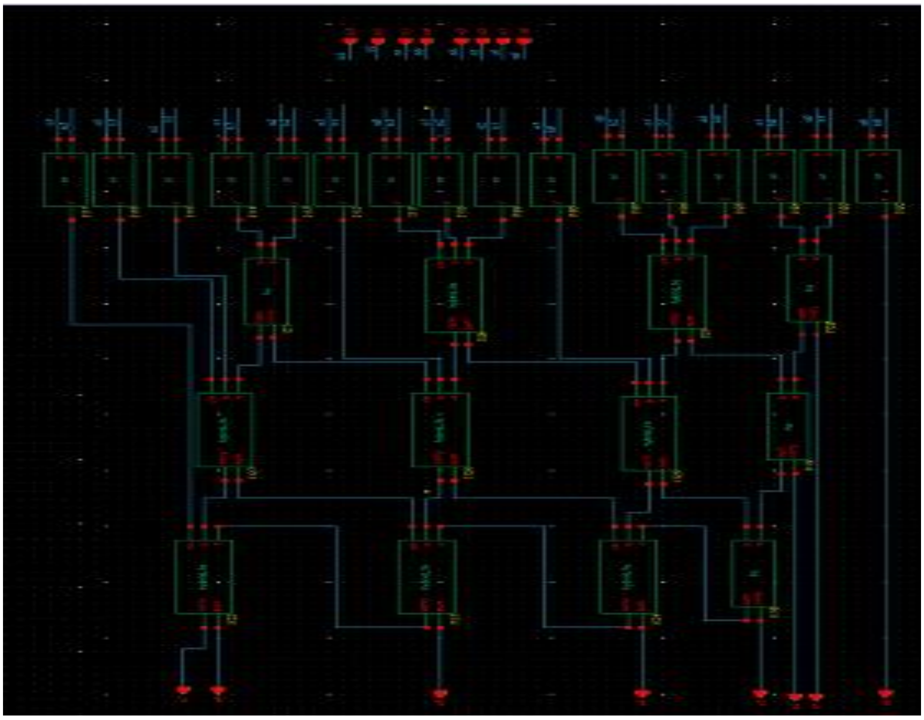

Figure 5. Wallace tree Multiplier using proposed hybrid GDI-PTL

Due to its parallelism and reduced propagation delay, the Wallace Tree architecture is particularly suited for real-time image and video compression, where speed and power efficiency are crucial. Integrating this multiplier into DCT computation blocks allows for faster coefficient generation and improved throughput, directly impacting compression speed and energy efficiency. However, traditional CMOS implementations of Wallace Tree multiplier consume considerable power and occupy generation embedded and portable multimedia applications. Multiplier structure is presented in Figure 4. to demonstrate the usefulness of the suggested AND, half adder, and full adder.

4. Experimental Results and Discussion

The proposed multiplier architecture, along with its fundamental building blocks namely the Half Adder and Full Adder circuits have been designed, implemented, and simulated using the Cadence EDA tool environment at both 90 nm and 45 nm CMOS technology nodes. A uniform supply voltage of 1.2 V has been employed across all simulations to ensure consistency in the evaluation process. To validate the efficiency of the proposed designs, extensive performance 1–4, highlight key performance parameters such as power consumption, propagation delay, and transistor count for Half Adders, Full Adders, and Wallace Tree multipliers. systematically compared with those of existing conventional logic styles. The comparative findings, summarized in Tables. These results clearly demonstrate the advantages of Furthermore, the simulation results of the proposed circuits are depicted in Figures 6–8, highlighting the functional correctness and illustrating the optimized design strategies adopted for the Half Adder, Full Adder, and Multiplier architectures. analysis has been carried out, and the results are the proposed methodology in terms of low-power and high-performance design, making it highly suitable for modern VLSI applications.

A. Transient Analysis of Half Adder

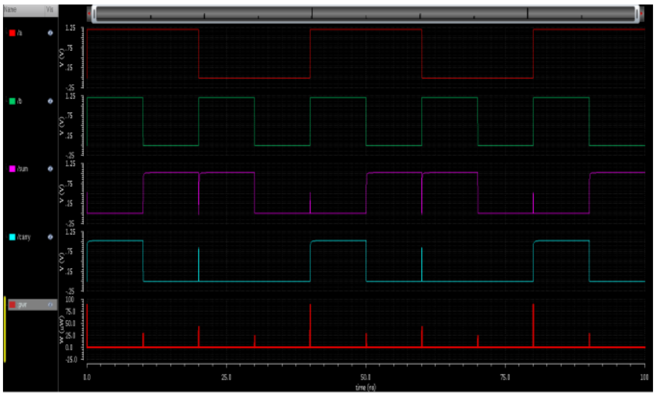

Figure 6. Simulation result of proposed half adder with power evaluation

B Transient Analysis of Full Adder

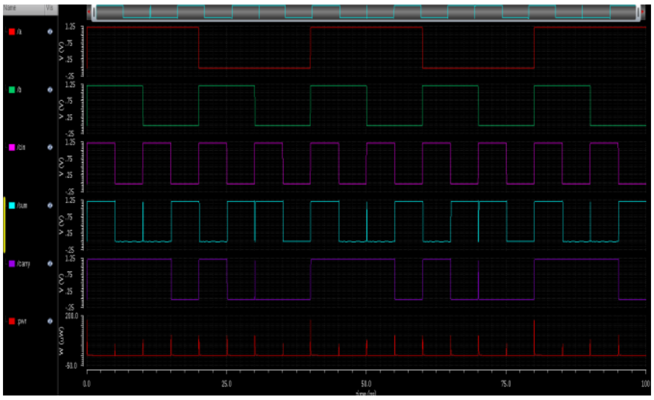

Figure 7. Simulation result of proposed hybrid Full Adder with power evaluation.

C. Transient Analysis of Wallace Tree Multiplier

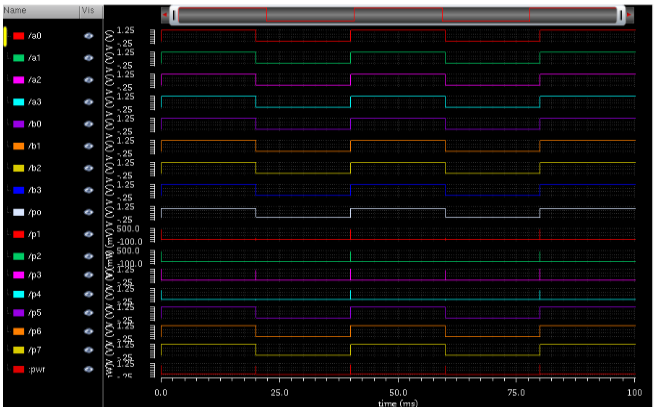

Figure 8. Simulation result of Wallace tree multiplier with power evaluation

Table 1. Comparison result of Half Adder

Parameter	PTL HA 90nm [5]	PTL HA 90nm [6]	Proposed GDI HA 90nm	PTL HA 45nm [6]	Proposed GDI HA 45nm
CMOS Technology node (nm)	90	90	90	45	45
Supply voltage (v)	1.2	1.2	1.2	1.2	1.2
Delay(ps)	2090	18.85	15.72	31.58	27.09
Power consumption (nw)	1105	247.2	76.52	48.12	25.24

Number of transistor Count	10	8	6	8	6

From the Table 1, we can observe that GDI based half adder has comparatively less power consumption compared to PTL only based half adder. Hence, it is chosen in designing the full adder circuit and in turn designing in Wallace tree multiplier circuit. The full adder design using PTL only technology, GDI technology,10T GDI based technology and hybrid PTL-GDI technology for reduced transistor count, power and delay are presented in table.

Table 2. Comparison results of Full adder using various Technology node

Parameter	PTL FA[5]	PTL FA[6]	Proposed GDI FA	Hybrid (GDI-PTL) FA	Proposed 10T GDI FA	PTL FA 45nm[6]	Proposed GDI FA 45nm	Proposed Hybrid (GDI-PTL) FA 45nm	Proposed 10T GDI FA 45nm
CMOS Technology node(nm)	90	90	90	90	90	45	45	45	45
Supply voltage (v)	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2	1.2
Delay(ps)	2140	23.59	18.55	21.13	22.28	62.88	20.02	21.20	23.10
Power consumption(nw)	1094	657.6	301	327.9	233.1	148.2	83.89	84.80	44.15
Number of transistor Count	18	18	14	10	10	18	14	10	10

Table 2 presents a comparative analysis of different full adder (FA) architectures implemented using various design methodologies such as GDI, PTL, Hybrid GDI-PTL, and conventional CMOS, across 90 nm and 45 nm CMOS technology nodes**.** The comparison is carried out based on three primary performance parameters: delay, power consumption, and transistor count**,** while maintaining a constant supply voltage of 1.2V.

Table 3. Comparative Evaluation of 90 nm Wallace Tree Multiplier Architectures Based on Logic Style Optimization

Work	Architecture	Logic Style	Tech (nm)	VDD (V)	Transistor Count	Delay	Power	Swing Restoration
D. B. R. et al.[5]	PTL Wallace	PTL	90	1.2	288	61.22 ns	55.86 µW	No
K. B. B. et al.[6]	PTL Wallace	PTL	90	1.2	240	18.03 ps	18.19 µW	No
Usha et al.[7]	EAI Wallace	CMOS	90	1.2	240	38 ns	6.92 mW	Yes
Proposed Work	GDI Wallace	GDI	90	1.2	168	12.61 ps	50.88 µW	Yes
Proposed Work	Hybrid GDI–PTL Wallace	Selective Hybrid	90	1.2	136	12.60 ps	37.94 µW	Yes
Proposed Work	10T GDI Wallace	GDI	90	1.2	136	12.60 ps	42.60 µW	Yes

Table 3 presents a comprehensive comparison of Wallace Tree multiplier implementations in 90 nm CMOS technology across different logic styles, including PTL-based, CMOS-based, pure GDI, and the proposed Hybrid GDI–PTL architectures. The comparison is carried out in terms of transistor count, propagation delay, power consumption, and output swing restoration capability. The PTL-based Wallace multipliers reported by D. B. R. *et al.* and K. B. B. *et al.* demonstrate reduced power consumption but exhibit either excessive delay or lack of full-swing restoration, which affects scalability and signal integrity. The CMOS-based EAI Wallace implementation provides reliable full-swing outputs but incurs significantly higher power dissipation and transistor count due to complementary pull-up and pull-down networks. In contrast, the proposed GDI-based Wallace multiplier substantially reduces transistor count and improves delay performance while maintaining full-swing operation. Among all implementations, the proposed Hybrid GDI–PTL Wallace multiplier achieves the most balanced performance, offering the lowest transistor count (136), minimal delay (12.60 ps), reduced power consumption (37.94 µW), and embedded swing restoration. This confirms that the selective hybrid integration effectively minimizes critical-path latency and switching losses while preserving signal integrity. Overall, the results validate the superiority of the proposed hybrid architecture over conventional PTL, CMOS, and standalone GDI implementations for low-power, high-speed multiplier design in deep-submicron VLSI systems.

Table 4 extends the comparison to 45 nm CMOS technology node, again at a supply voltage of 1.2 V. At this scaled technology all three proposed architectures **(**GDI WTM, Hybrid GDI-PTL WTM, and GDI-10T WTM**)** achieve the same delay of 27.76 ps, indicating that performance is now dominated by technology scaling rather than circuit style. In terms of power consumption, the Proposed GDI WTM achieves the lowest value **(**8.045 µW**)**, making it the most energy efficient.

The Hybrid GDI-PTL WTM consumes 10.57 µW, while the 10T GDI WTM records the highest power (14.52µW). Regarding area, both the Hybrid GDI-PTL and 10T GDI WTM use only 136 transistors**,** making them more compact compared to the GDI WTM (168 transistors). Hence, at 45 nm technology, the GDI WTM offers superior power efficiency, whereas the Hybrid GDI-PTL and 10T GDI WTMs provide area efficiency. This confirms that GDI-based multiplier architectures remain effective even in deep sub-micron technologies**,** ensuring low-power and compact designs suitable for high-performance image compression applications energy-efficient. The Hybrid GDI-PTL WTM consumes 10.57 µW, while the 10T GDI WTM records the highest.

Table 4: Comparison results of Wallace Tree multiplier using 45nm Technology node

Parameter	Proposed GDI- Wallace tree multiplier	Proposed Hybrid (GDI-PTL) Wallace tree multiplier	Proposed GDI-10T Wallace tree Multiplier
CMOS Technology node (nm)	45	45	45
Supply voltage (v)	1.2	1.2	1.2
Delay(ps)	27.76	27.76	27.76
Power consumption (µw)	8.045	10.57	14.52
Number of transistor count	168	136	136

Table 5: Performance Comparison of different Logic styles

Logic styles	Delay	Power Consumption	Power–Delay Product (PDP)
CMOS [12]	0.80 ns	7.84 mW	6.27 pJ
PTL[5]	61.22 ns	55.86 µW	3.42 pJ
GDI	12.61 ps	50.88 µW	0.64 fJ
Hybrid GDI-PTL	12.60 ps	37.94 µW	0.48 fJ

Table 5 clearly demonstrates that the proposed Hybrid GDI–PTL logic style achieves the most efficient power–performance trade-off among all evaluated designs. While conventional CMOS shows high robustness, it suffers from significantly higher power dissipation and PDP due to large switching capacitance. PTL reduces power but exhibits excessive delay caused by threshold voltage degradation. Pure GDI considerably improves speed with low power; however, the proposed Hybrid GDI–PTL further optimizes both metrics simultaneously, achieving the lowest delay and minimum PDP. This confirms that the selective integration of GDI and PTL effectively minimizes critical-path delay and switching losses, making the hybrid approach superior for high-speed, low-power arithmetic applications.

5. Performance Comparison of Wallace Tree Multiplier Designs

To evaluate and compare the efficiency of various Wallace Tree multiplier designs, comprehensive analyses were performed on three key performance parameters: delay**,** power consumption, and transistor count**.** The results are illustrated in Figures 9,10 and 11.

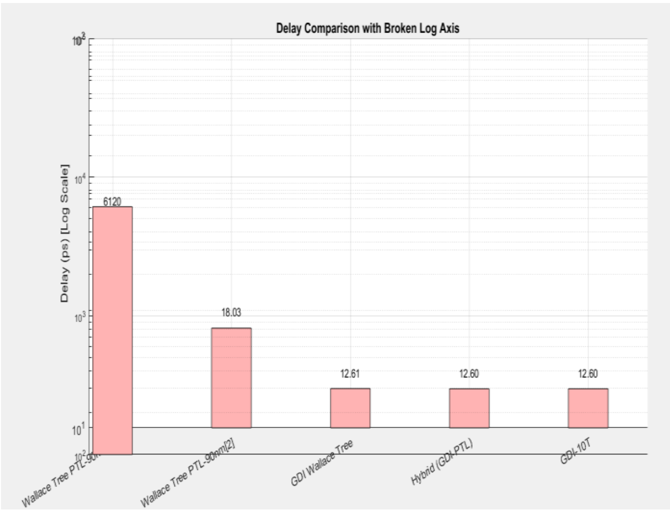

Figure 9. Timing comparison of Wallace Tree multiplier

Figure 9 presents the delay comparison on a logarithmic scale, where the [1] Wallace Tree using pure PTL at 90nm exhibits an exceptionally high delay of 6120 ps, highlighting the limitations of PTL-only structures at older technology nodes. In contrast, all other designs including the [2] PTL Wallace Tree, GDI Wallace Tree, Hybrid GDI-PTL design, and GDI-10T achieve significantly reduced delays, clustered around 12–18 ps, demonstrating improved performance and suitability for high-speed applications.

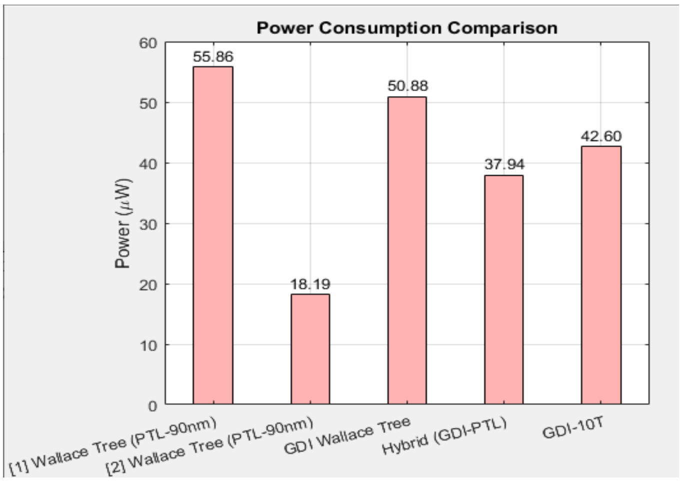

Figure 10. Power consumption comparison of Wallace Tree multiplier architectures

Figure 10 shows the power consumption comparison. The proposed Hybrid GDI-PTL and GDI-10T designs offer a balanced trade-off, maintaining moderate power consumption values of 37.94 µW and 42.60 µW, respectively, while still ensuring performance benefits. The conventional PTL and GDI Wallace Tree implementations show higher power dissipation, peaking at 55.86 µW.

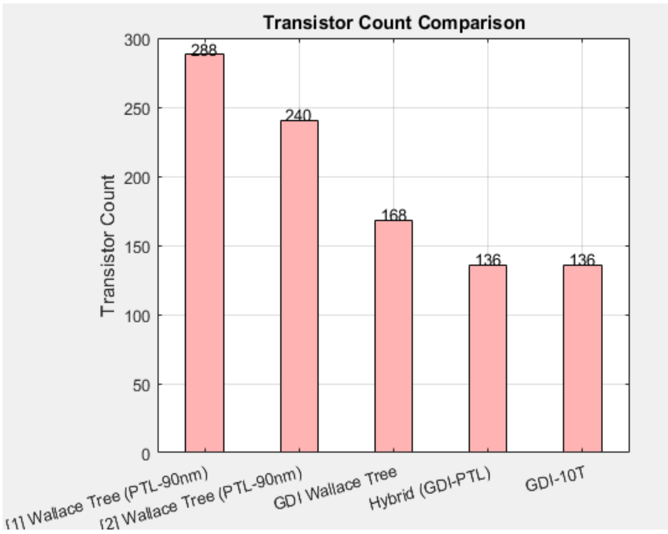

Figure 11. Transistor Count analysis of Wallace Tree multiplier architectures

Figure 11 illustrates the transistor count analysis. The GDI 10T and Hybrid (GDI-PTL) designs demonstrate significant area savings with the lowest transistor count of 136, followed by the GDI Wallace Tree (168 transistors). In contrast, traditional PTL-based Wallace Trees consume up to 288 transistors, reflecting the design inefficiencies in terms of area and complexity. These comparative results validate the efficacy of the proposed Hybrid GDI-PTL architecture, showcasing substantial improvements in speed, area, and power, making it an optimal solution for low-power VLSI applications, GDI-PTL logic style, targeting low-power image processing applications. The proposed Hybrid Wallace Tree Multiplier, which integrates the compactness of Gate Diffusion Input (GDI) with the high-speed benefits of Pass Transistor Logic (PTL), achieves superior results in terms of power, delay, and area. Among all evaluated designs in 90nm technology, the Hybrid (GDI-PTL)-based Wallace Tree Multiplier achieves a significant reduction in delay, registering just 12.61 ps, which is a substantial improvement over the 61.22 ns delay observed in the conventional PTL only-based implementation and conventional CMOS implementation. While its power consumption of 50.88 µW is marginally higher than that of the PTL[2]-based design **(**18.19 µW**),** it remains significantly lower than traditional CMOS and PTL **(**55.86 µW**),** with the benefit of reduced delay and optimized performance.

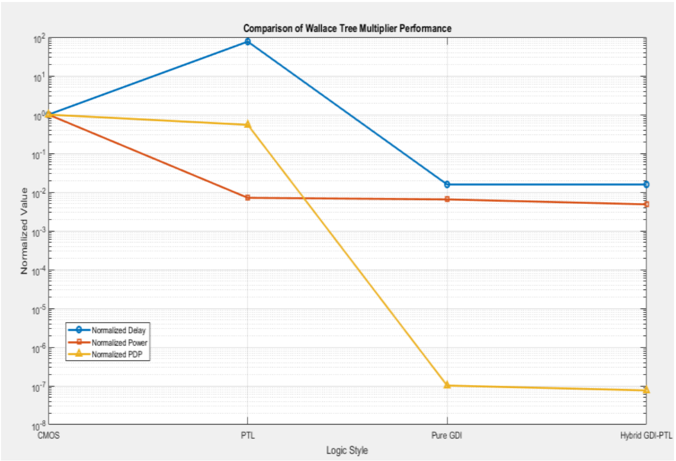

Figure 12. Log-normalized composite performance comparison of Wallace Tree Multiplier implementations using CMOS, PTL, Pure GDI, and Hybrid GDI–PTL logic styles at 90 nm technology

5. Conclusion

This proposed work presents a comparative analysis and implementation of various Wallace Tree Multiplier architectures using CMOS, GDI, and a proposed Hybrid GDI-PTL logic style, targeting low-power image processing applications. The proposed Hybrid Wallace Tree Multiplier, which integrates the compactness of Gate Diffusion Input (GDI) with the high-speed benefits of Pass Transistor Logic (PTL), achieves superior results in terms of power, delay, and area. Among all evaluated designs in 90 nm technology, the Hybrid (GDI-PTL)-based Wallace Tree Multiplier achieves a significant reduction in delay, registering just 12.61 ps, which is a substantial improvement over the 61.22 ns delay observed in the conventional PTL only-based implementation and conventional CMOS implementation. While its power consumption of 50.88 µW is marginally higher than that of the PTL[2]-based design **(**18.19 µW**),** it remains significantly lower than traditional CMOS and PTL **(**55.86 µW**),** with the benefit of reduced delay and optimized performance.

In terms of area, the proposed hybrid design uses only 136 transistors, offering a substantial reduction from the 288 used in the baseline CMOS PTL design and even outperforming other GDI variants. The transistor count and layout compactness directly contribute to lower parasitic capacitance and power savings. The 45 nm implementation of the Wallace Tree Multiplier further validates the scalability of the hybrid approach, achieving an ultra-low power consumption of 10.57 µW, demonstrating its potential for integration into energy-constrained, high-performance systems such as portable image processors, IoT edge devices, and mobile medical imaging platforms. In summary, the Hybrid GDI-PTL Wallace Tree Multiplier offers a highly efficient trade-off between power, performance, and area, making it well-suited for real-time DCT-based image compression and other high-speed digital signal processing applications.

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