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Review of Network on Chip Routing Algorithms

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Abstract

System on chip (SoC) is an integrated circuit in which components are communicating through the bus interconnection system. Network on chip (NoC) is a communication network for a multiprocessor system on chip (MPSoC). In NoC architecture node/ component of MPSOC are communicating through a network. The performance of NoC architecture depends on topology, routing algorithm and switching technique. In this paper, different NoC routing algorithms are review using basic parameters of NoC architecture and also provide some information about these parameters. It is concluded that most of the researchers are interested in design of the NoC routing algorithm, which efficiently transmits data from source to destination. When the routing algorithm is congestion aware, fault-tolerant, deadlock-free and live-lock free, then the latency of algorithm decreases and throughput increases.

Keywords: System on Chip, Network on Chip, Routing Algorithm.

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1. Introduction

The System on Chip (SoC) has a prominent role in the computing world. It is used in mobile computing, embedded system and now also implied to a personal computer such as laptop and tablet PC etc. SoC is a design methodology used by very-large-scale integration (VLSI) designers. The interconnection system of SoC based on share bus or dedicated bus. The basic problem in the bus system as that it allows one communication at the time [1]. Advancement in technology, SoC in an embedded system is increasingly large and complex [2]. Fig (1) shows the interconnection system of SoC in which different devices are connected through a shared bus system. The problem of communication arises because bus architecture cannot meet the requirement like area utilisation, single clock synchronisation, propagation delay, latency, throughput and power consumption [3]. Network on chip (NoC) appear as a better solution for the implementation of SoC [1]. NoC can be defined as "*A communication network targeted for on-chip communication*". NoC is efficient for on-chip communication for SoC [4-6].

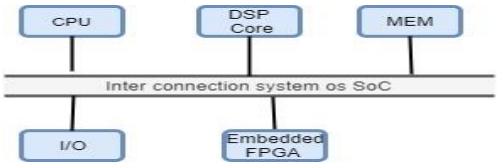

Fig (1). Interconnection System of SoC

NoC is a communication network between multiple devices. Devices are connected in regular or irregular topology [7-9]. The devices are processor, memory, DSP core etc are called processing element (PE). The PE has two types, homogeneous and heterogeneous. Fig (2) shows 4*4 mesh topology of NoC. In which PEs are connected to local routers through a network interface (NI) and routers are connected to each other with a point to point connection. The NI transforms the message to packet and packet received by router send it to neighbour router. The packet move to the destination is travelling through routers [10, 11].

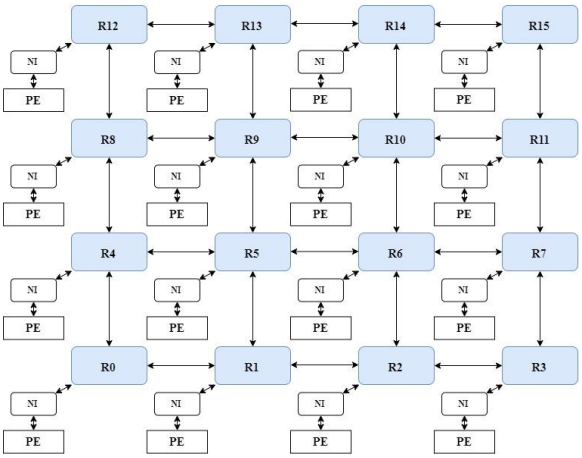

Fig (2). 4*4 NoC

The overall performance of NoC depends on topology, routing algorithm, flow control and switching technique [4]. Topology means how nodes are connected in a network. There are different types of topology such as mesh, torus, tree, ring, star, spidergon and also some irregular topology [10]. Routing algorithm defines the path taken by a packet from source to destination. XY, IX/Y, XYX etc. are some example of routing algorithm [4]. There are two major types of switching, circuit switching and packet switching. In circuit switching a physical or virtual link are establishing between source and destination. In packet switching message is divide into packets at source and routed to the destination. The routing algorithm determines a route for packet [3]. The understanding of routing algorithm is very critical in designing of NoC architecture.

Routing algorithms is a key factor affecting NoC network communication. In this review, we compare different routing algorithm on the bases of a basic parameter of NoC architecture. The parameter for the comparison of routing algorithm are topology, routing type, switching technique, packet and flit size, power dissipation, latency, throughput and simulator on which routing algorithm are implemented. The comparison of routing algorithms is shown in Table 1. We believe that this review paper is helpful for the researcher community to resolve routing issue of NoC architecture in future.

The remainder of the paper is organised in such a way that in section 2, we define deadlock, live-lock and starvation situation of routing algorithms. In section 3, different types of routing algorithm are discus. In section 4, we discussed topology and its type. In section 5, we discussed switching technique and also which switching technique is used in the implementation of which routing algorithm. In section 6 and 7, we discussed which one algorithm is congestion aware and which one is fault-tolerant. In section 8, the power dissipation of review routing algorithms is the discus. In section 9, latency and through are discus. In section 10, we discussed different simulator on which the review routing algorithms are implemented.

2. Contemplation on the routing algorithm

Every routing algorithm has a different impact on different NoC architecture. It affects different properties of NoC architecture such as latency, throughput and power consumption.

The routing algorithm is similar to routing in any network. Routing algorithm decides path followed by a packet in communication from source to destination [1, 12, 13]. They prevent deadlock, live-lock and starvation situation. Deadlock is cyclic dependency among node making access to resources where no progress can be made. Live-lock as refers to a situation where packet circulates in the network but not reaching to the destination. In starvation packet in buffer request for output channel but output channel also allocated to another packet [1].

3. Routing type

Different types of routing algorithms are developed for the designing of NOC. Routing algorithms are classified on three key characteristics. Which are routing decision, defining path and path length [1, 12]. On the base of the routing decision, there are two types of source and distributed routing. In source, routing path defines by source router and in distributed routing, each router decides the next direction for packet [1]. According to path defining or adaptively, the routing algorithm has two type deterministic and adaptive algorithms. The path is completely determined from source to destination in advance in the deterministic algorithm. There also as another type partially adaptive which restrict some direction [13]. On the base of path length, there are two types minimal and non-minimal. Shortest path selection algorithm is minimal and the longest path selection algorithm is non-minimal [1, 13].

The routing algorithms GOAL, GAL, DyXY, BARP, ADBR, MaS, Fault-tolerant, FAFT, FT-DyXY, Free-rider, Novel Adaptive, Traffic allocator, MCAR, Efficient deadlock-free, ESPDA and Adaptive multipath are adaptive routing algorithm [9, 14-28]. OE and 3DEP are partial adaptive routing algorithm [29, 30]. DyAD and FA-DyAD are adaptive and deterministic [31, 32]. The deterministic routing algorithms are FTXY and ZigZig [33, 34]. Some more classification is possible like congestion aware algorithm, and Fault-Tolerance-routing algorithm will discuss in section 6 and 7.

4. Topology

Topology in NoC is an organisation of router and channel. Topology is the roadmap for communication of PE in NoC [35]. It's divide into two types [10]. In regular topology, nodes are connected in a specific pattern. Mesh, torus, star,

ring and tree are popular regular topology [10, 35-38]. The mash topology has M rows and N columns. The intersection of row and column consists of routers and the router are connected to its neighbours. Tours topology are similar to mesh but end routers are connected together with the same row and column routers. In star topology, all routers are connected to a central router. The router is connected to its two neighbours circle shape are ring topology. In tree topology, a child router is connected to its parent router. Fig (3-6) shows the structure of torus, star, ring and tree topology. In irregular, topology nodes are not connected in fix pattern. Fig (7) shows irregular topology.

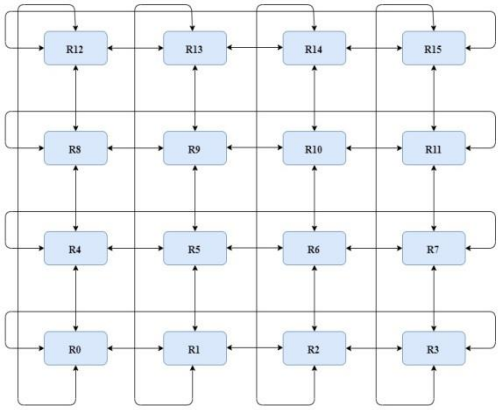

Fig (3). Torus topology

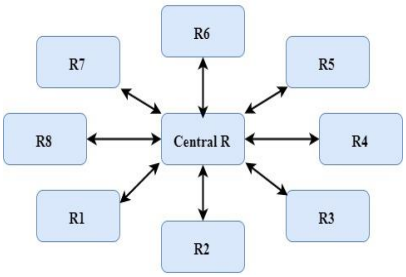

Fig (4). Star topology

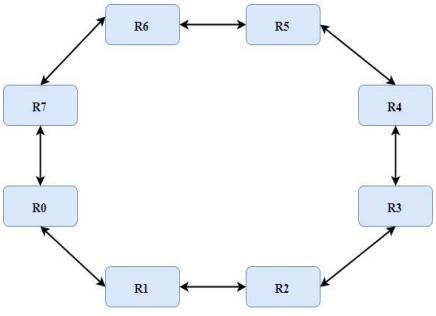

Fig (5). Ring topology

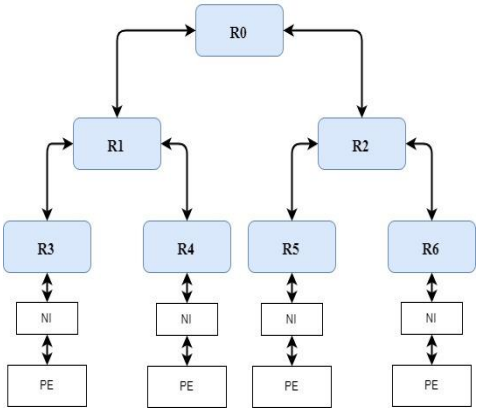

Fig (6). Tree topology

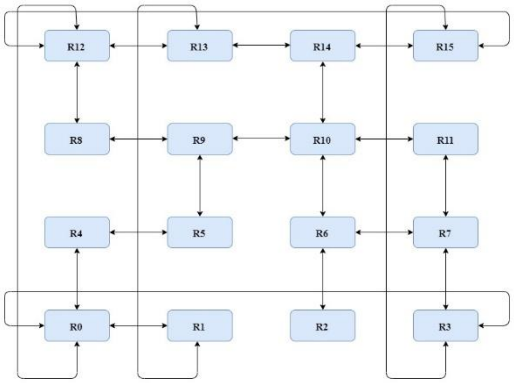

Fig (7). irregular topology

To design the routing algorithm for the network, the choosing of topology is the principle step. The performance of the routing algorithm depends on the topology on which it's implemented and also on the number of routers in the topology. When the same algorithm is implemented on mesh 4×4, and mesh 8×8 have different performance [28]. O1TURN [39], DyXY [16], BARP [18] and FT-XY [33] are implemented on mesh topology having a different number of the router. In this review, Table 1 shows that most of the routing algorithm is implemented on a mesh topology.

Table 1. NoC Routing algorithm

S.NO	Algorithm	Compression Parameters									
		Year	Topology	Routing Type	Routing characteristic	Switching technique	Packet and flit Size	Power dissipation	Latency	Throughput	Simulator
1	OE [29]	2000	15×15 2D mesh	Partial adaptive	Deadlock free	-	-	-	-	-	Event-driven simulator
2	GOAL [14]	2003	Torus	Adaptive	-	-	-	-	-	-	Cycle accurate network simulator
3	GAL [15]	2004	8×8 Torus	Adaptive	Congestion aware	Wormhole	-	-	-	-	Cycle accurate network simulator
4	DyAD [31]	2004	6×6 2D mesh	Deterministic and Adaptive	Congestion aware and Deadlock free	Wormhole	-	-	-	At injection rate 0.0167 are 0.027 packet/cycle	Worm_sim simulator
5	O1TURN [39]	2005	4×4, 8×8 2D mesh	-	Deadlock free	-	5 Flit	-	-	-	PoPnet simulator
6	DyXY [16]	2006	3×3, 9×9 2D mesh	Adaptive	Congestion aware, deadlock-free and live-lock free	-	-	-	At Average injection rate of 0.3 are 14 Approx.	-	Event-driven simulator using C++
7	Fault aware dynamic routing [40]	2008	4×4 2D mesh	-	Fault-tolerant	Cut through	4 flit	-	When 2 fault, injection rate 20 flit/node/cycle then 78 cycle	-	MATLAB Simulink
8	BARP [18]	2008	8×8, 14×14 2D mesh	Adaptive	Deadlock and live-lock free	Wormhole	Flit is 16 bit	-	Injection rate .25 message/cycle then 400 cycle	-	Developed on flit level NoC simulator using C++
9	IX/Y [41]	2008	2D mesh	Adaptive	Deadlock free	-	-	-	At injection	-	Noxim

									rate .05 then below 30cycle		
10	ADBR [17]	2008	8×8 2D mesh	Fully adaptive	Deadlock free and flow control	-	-	0.00035 J	at injection rate 0.03 are 250 cycle	0.175 flit/cycle	Noxim
11	XYX [42]	2009	2D	Deterministic	Fault tolerant	-	32 flit	-	-	-	VHDL based NoC simulator
12	FT-XY [33]	2009	5×5, 6×6 2D mesh	Deterministic	Deadlock free	-	-	For 6×6 Injection rate 0.005-0.009 packet/cycle/node are 0.02-0.09 J	For the 6×6 Injection rate, 0.03 are 85 cycle Approx.	-	Noxim
13	DBFA LCI [43]	2009	4×4×4 3D Torus	-	Live-lock free, Asynchronous.	-	-	-	-	-	OPNET
14	EDXY [44]	2010	7×7, 15×15 2D mesh	-	Congestion aware	-	-	For 15×15 injection rate 9% then 26.1197	For 7×7 In uniform traffic injection rate 28% then 100 cycle	-	VHDL
15	FA-DyAD [32]	2010	6×6 2D mesh	Deterministic and adaptive	Fault and congestion aware	-	-	-	Fault 10%, injection rate .08 packet/cycle then 630 approx.	-	gpNocsim
16	Low latency routing algorithm [45]	2011	3D consist of 4×4 2D mesh layer	-	-	-	-	-	-	-	Xilinx 10.1 version is used for simulation of results
17	MaS routing [19]	2012	10×10 mesh	Adaptive, buffer less	Live-lock free	Wormhole	8 flit and 128 bit	At injection rate of 0.21 Flit/cycle/node are 6.5w	Average latency of 53 cycle		On-chip network simulator
18	Fault-tolerant	2012	8×8 2D mesh	Adaptive	-	-	16 flit and 128 bit	-	-	-	XMulator

	routing [9]										
19	CATRA [46]	2012	8×8, 14×14 2D mesh	-	Congestion aware	-	1-5 flit distributed uniformly	2.51w	At injection rate 0.35 f/n/c are 200 cycle	-	Implemented through VHDL
20	Preconcerted wormhole routing [47]	2012	-	-	Based on the virtual circuit	wormhole	-	-	-	-	NIRGAM
21	FAFT routing [20]	2013	4×4×3 3D mesh	Fully adoptive	Fault-tolerant	-	-	-	-	-	Noxim
22	FT-DyXYZ [21]	2014	3D mesh	Adaptive	Fault-tolerant	-	5 flit	-	-	-	Booksim
23	Free-Rider [22]	2014	16×16 2D mesh	Adaptive	Congestion aware		5 flit and 128 bit				Booksim
24	Novel adaptive routing [23]	2015	8×8×4, 16×16×13D mesh	Adaptive	Congestion aware	-	-	At injection rate 0.5 are 1	At injection rate 0.5 are 1	At injection rate 0.5 are 1	Noxim
25	Distance prediction XY [48]	2015	2D mesh	-	-	-	2-10 flit	-	-	-	System C platform
26	DRTL [49]	2016	4×4×4 3D mesh	-	Deadlock free	Wormhole	5 flit and 64 bit	-	-	-	Alpha EV6 core model is used result simulation
27	Traffic allocation routing [24]	2016	6×6 2D mesh	Adaptive	-	-	A packet is 20 bytes	When load 50% then 61.973 mw	When load 50% then 45.9084 cycle/flit	-	NIRGAM
28	MCAR [27]	2017	8×8, 16×16 2D mesh	Adaptive	Congestion aware	-	-	7.85% on average	-	5.84% on average	Booksim 2.0
29	Efficient deadlock-free adaptiv	2017	4×4×4, 8×8×4 3D mesh	Adaptive	Dead lock-free	-	A packet is 8 bit	-	-	-	Noxim

	e [26]										
30	ESPA DA [25]	2017	8×8 2D mesh	Fully adaptive based on virtual channel	Dead lock-free	-	5 flit and 64 bit	-	-	-	GPU based on cyclic accurate NoC
31	ZigZig [34]	2017	2D mesh	deterministi c	-	-	Packet is 20bytes	The load is 50% then 62.698 mw	Average latency is 46.2517 cycle/fli t	-	NIRGA M
32	Adapti ve multip ath [28]	2018	4×4, 8×8 2D mesh	Adaptive	Congestion aware	-	8 flit and 32 bit	-	For 4×4 Load 0/9 GB/sec 330 Ns	-	HNOC based on OMNET ++
33	Link-Sharin g [50]	2018	8×8 2D mesh	-	Congestion aware	Wormhole	Flit is 32 bit	2.86 mw	-	-	RTL level by using VHDL
34	UMF [51]	2019	Mesh	-	Dead lock free	-	5 flit	-	-	-	PopNet
35	TBTF TA [52]	2019	8×8 2D mesh	-	Congestion aware, thermal-fault tolerant	-	-	-	-	Offer load increas es high throug hput	OPNET
36	3DEP [30]	2019	3D mesh	Partially adaptive	Dead lock free	-	-	-	-	-	Noxim
37	CFPA [53]	2019	Mesh and torus	-	Congestion aware, fault-tolerant	-	-	-	-	-	HNOC for algorithm and MC used for circuit-level delay

5. Switching Technique

Switching technique refers to the flow control mechanism of messages between routers. The basic switching techniques that are used in NoC is circuit switching and packet switching. Packet switching is further divided into three broad categories wormhole, store and forward and virtual cut through [10, 54]. In the wormhole, the packet is divided into flit (head flit, body flit and tail flit). Head flit contains source and destination information, body flit contains data which is transmitted to destination and tail flit contain ending information of flit. Due to the pipelined nature of wormhole, it redacts message latency [31, 54, 55]. In store and forward technique, the whole packet is store in the router then routed to the next router. In virtual cut through, the packet is forwarded to the next router if it ensures that the whole packet is store in it [10, 54].

Due to pipeline nature and low latency wormhole switching technique are preferring in designing of routing algorithm. The GAL, DyAD, BARP, MaS, Preconcerted wormhole routing, DTRL and Link sharing are implemented using wormhole switching technique [15, 18, 19, 31, 47, 49, 50].

6. Congestion Awareness

It's characteristic of routing algorithm which improves the performance of NoC by distributing the load over network

and send the traffic over the less congested area. On congestion awareness basis routing algorithm are divided into two types. Congestion oblivious algorithm and congestion aware algorithm [46, 56]. Congestion oblivious algorithm is unable to balance the load over the network and can't consider the congestion status of the network. Without congestion awareness interconnection system of the network is unbalanced and burst. On the other hand, the congestion aware algorithm routes the traffic through the largest available virtual channel.

Table 1 show that GAL, DyAD, DyXY, BARP, EDXY, FA-DyAD, CATRA, Free-Rider, Novel adaptive routing, DTRL, MCAR, Adaptive multipath, Link sharing and CFPA are congestion aware algorithms [15, 16, 20, 22, 27, 28, 31, 32, 44, 46, 50, 52, 53]. Congestion awareness decrees latency and increases throughput. Congestion aware algorithms are further divided on the base of sharing of congestion information are local and non-local [22].

7. Fault tolerance

Fault tolerance is network property to examine the functioning of the network component and remains its functioning when some components are inactive/faulty. Fault can occur as a result of a defect in the system, improper environment and improper design of a system. Fault in NoC is categories in two groups on the base of time and occurrence. Hardware fault occurs due to hardware fault of the system and for its removing extra hardware or resources are required [57-59]. The soft fault is denoted by a bug in the software and it can be addressed by routing algorithm.

Scientists and researchers propose different fault-tolerant routing to overcome fault in NoC [10, 60]. A routing algorithm for fault tolerance is Fault aware dynamic routing, FA-DyAD, FAFT routing, FT-DyXY, TBTFTA and CFPA [20, 21, 32, 40, 52, 53]. The compression of these algorithms is shown in table 1.

8. Power Dissipation

In the designing of the routing algorithm, the power dissipation is under consideration of scientists and researchers. Power dissipation is divide into two parts; static and dynamic. Static power relates to manufacturing technology and dynamic power depends on the router activity [61]. In [62-66] are the technique are proposed to reduce power consumption.

The power consumption of FT-XY under uniform traffic of 4×4 NoC is .01 to .09 J and for 6×6 NoC its .02 to .09 J for injection rate of .005 to .019 packet/cycle/node [33]. The power consumption for ADBR is .00035J, for MaS algorithm it's a 6.5w at injection rate of 0.21 packet/cycle/node, for Traffic allocation routing algorithm it's 61.973mw when load is 50%, for ZigZig algorithm it's 62.698mw when load is 50% and for Link sharing algorithm it's 2.86mw [17, 19, 24, 34, 50].

9. Latency and Throughput

The performance of the routing algorithm depends on latency and throughput. The performance of routing is batter when its latency is low, and throughput is high. Most of the researchers compare their own proposed routing algorithm latency and throughput with other routing algorithms for performance evaluation. Throughput of CFPA is compared with XY and DyAD and shown that its throughput is better than XY and DyAD [53].

The latency and throughput of routing algorithm depend on the number of tiles in NoC, e.g. for same algorithm latency and throughput for 4×4 and 8×8 are different. When the number of tiles in NoC increases the latency of routing algorithm increase and throughput is decrees [23, 28, 34, 44]. Latency and throughput of routing algorithm also depend on the injection rate [16, 18, 32, 40]. Latency and throughput of the review routing algorithms are shown in Table 1.

10. Simulator

There are three approaches for the to evaluate the performance of the system

- Actual system monitoring
- Mathematical modelling
- Simulation modelling

The simulation environment provides an extensible framework for NoC evaluation and provides more feature, different topology, swathing technique, routing algorithm, flow control polices and high accuracy [67-69].

In this review, Table 1 shows most of the routing algorithm performance is evaluated on Noxim, Booksim and NIGRAM simulator. Noxim simulator is used for the performance evaluation of ADBR, FT-XY, FAFT routing algorithm, Novel adaptive routing, Efficient deadlock-free adaptive routing and 3DEP. Booksim simulator is used for FT-DyXY, free-rider and MCAR. Precocerted wormhole routing, traffic allocation routing and ZigZig routing algorithm performance are evaluated through NIGRAM simulator. Some other simulator Event-driven, XMultar, PopNET, gpNoCsim, OpNET, Matlab simulator and event-driven are used for performance evaluation of routing algorithms.

11. Conclusion

This paper review different routing algorithm of NoC on the base of different parameter. In our view, it's helpful for the researcher community to find and resolve the unanswered issue of this area. Based on Table 1, it is concluded that most of the researchers are interested in to design the routing algorithm, which has low latency, high throughput, low power consumption, congestion aware and fault-tolerant. From this review it is concluded that, in the designing of routing algorithm the designers/researchers should compromise on some parameters. When the

algorithm is congestion aware, fault- tolerant, dead lock free and live-lock free than power consumption, area utilisation and some other parameter like processing are increase but the latency is decrease and throughput is increase.

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