Book Titled *Autonomic Networking-on-Chip: Bio-Inspired Specification, Development, and Verification*: An Introduction

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Abstract

Despite the growing mainstream importance and unique advantages of autonomic networking-on-chip (ANoC) technology, Autonomic Networking-On-Chip: Bio-Inspired Specification, Development, and Verification is among the first books to evaluate research results on formalizing this emerging NoC paradigm, which was inspired by the human nervous system. The third book in the Embedded Multi-Core Systems series from CRC Press, this is an advanced technical guide and reference composed of contributions from prominent researchers in industry and academia around the world. A response to the critical need for a global information exchange and dialogue, it is written for engineers, scientists, practitioners, and other researchers who have a basic understanding of NoC and are now ready to learn how to specify, develop, and verify ANoC using rigorous approaches.

1. Introduction

A new networking-on-chip paradigm, which is seen as a cutting-edge approach to network-on-chip (NoC), is currently on the spot as one of the priority research areas: autonomic networking-on-chip (ANoC), which is inspired by the human autonomic nervous network.

ANoC is a networking-on-chip paradigm able to realize its self-* functionality such as self-organization, self-healing, self-configuration, self-optimization, self-protection, and so on whose context awareness is used to control networking functions dynamically. The overarching goal of ANoC is to realize intelligent networks-on-chips that can manage themselves without direct human interventions. Meeting this grand challenge of ANoC requires a rigorous approach to ANoC and the notion of self-*. To this end, taking advantage of formal engineering methods we will establish, in this book, formal and practical aspects of ANoC through specifying, refining, programming and verifying ANoC and its self-*. All of these are to achieve foundations and practice of ANoC.

From the above characteristics, novel approaches of specification, refinement, programming and verification are arising in formal engineering methods for ANoC. Therefore, new methodologies, programming models, tools and techniques are imperative to deal with the impact of ANoC and its self-* mentioned above on emerging intelligent networks-on-chips.

The book [1] is a reference for readers who already have a basic understanding of NoC and are now ready to know how to bio-inspiredly specify, develop and verify ANoC using rigorous approaches. Hence, the book includes both theoretical contributions and reports on applications. To keep a reasonable tradeoff between theoretical and practical issues, a careful selection of the chapters was completed, on one hand, to cover a broad spectrum of formal and practical aspects and, on the other hand, to achieve as much as possible a self-contained book.

Formal and practical aspects will be presented in a straightforward fashion by discussing in detail the
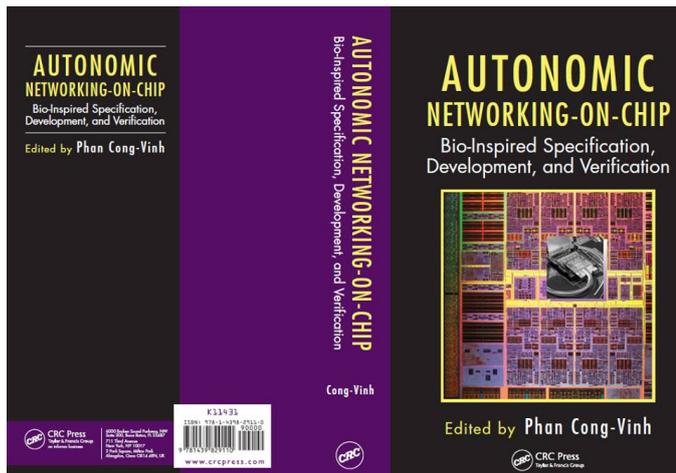

Figure 1. Cover of the book

necessary components and briefly touching on the more advanced components. Therefore, bio-inspired specification, development and verification demonstrating how to use the formal engineering methods for ANoC will be described using sound judgment and reasonable justifications.

This book, with chapters contributed by prominent researchers from academia and industry, will serve as a technical guide and reference material for engineers, scientists, practitioners and researchers by providing them with state-of-the-art research findings and future opportunities and trends. These contributions include state-of-the-art architectures, protocols, technologies, and applications in ANoC. In particular, the book covers existing and emerging research issues in bio-inspired on-chip networks (BioChipNets). The book has eight chapters addressing various topics from specification to implementation of ANoC based on rigorous interdisciplinary approaches.

2. Contents of the Book

Chapter 1 by M. Bakhouya presents an overview of state-of-the-art approaches for ANoC. Unlike design-time approaches in which all parameters/protocols are optimized/selected at design time targeting a specific application, in run-time approaches the adaptation process is running continuously to evolve the system. Based on this state-of-the-art review, the self-* capabilities are considered in the context of ANoC. These capabilities can provide the core scheme to develop ANoC at application, communication and architecture levels. An approach inspired by a biological immune system toward developing ANoC with these self-* capabilities is introduced. One aspect of the self-healing capability is partially developed, and some preliminary results are reported and showed that the adaptation is energy and latency efficient.

Chapter 2 by A. A. Morgan, H. Elmiligi, M. W. El-Kharashi, and F. Gebali discusses a GA-based multi-objective technique for autonomous on-chip network architecture optimization. This technique considers four NoC metrics: power, area, delay, and reliability. The models of the four metrics are discussed. The formulation of the fitness function is then presented. Finally, the GA representation of the problem is explained. The optimization can be carried out for power, area, delay, reliability or the four of them according to weight factors supplied by the designer. Results show that the technique is an efficient way to compromise between different NoC metrics. Moreover, the running time of the technique makes it more suitable for ANoC than previous architecture optimization techniques.

Chapter 3 by K. Latif, A. M. Rahmani, T. Seceleanu, and H. Tenhunen discusses an autonomous PVS-NoC architecture where an ideal tradeoff among virtual channel utilization, system performance and power consumption is presented. The virtual channel buffers are shared between two input ports in PVS-NoC. Apart from system performance, the architecture is also fault tolerant. In case of any link failure, the VC buffers are used by the other physical channel sharing the VC buffers, and system performance is not affected severely. The architecture is simulated with synthetic and real application traffic patterns. The performance is compared with typical VC-based NoC architecture and FVS-NoC. The PVS-NoC architecture shows significant improvement in system throughput without significant power consumption overhead.

Chapter 4 by J. Jaros and V. Dvorak discusses an evolutionary design that is able to produce optimal or near optimal communication schedules comparable to or even better than those obtained by a conventional design for the networks sizes of interest. Moreover, evolutionary design reduces many drawbacks of present techniques and invents still unknown schedules for an arbitrary topology and scatter/broadcast communication patterns.

Chapter 5 by P. C. Vinh breaks new ground in dealing with the *core-to-core* and *agent-based networking techniques* for ANoC using a categorical approach of tasks and data parallel processing – the firm formal method applicable to a wide variety of BioChipNets. The major contribution of the chapter is to propose some applied categorical structures of tasks parallel and data parallel for parallel processing on BioChipNets that has never been tackled thoroughly in this emerging field. By this approach, category theory is applied to deal in an abstract way with algebraic objects and relationships between them for specifying tasks parallel and data parallel on BioChipNets. The chapter shows that for specifying, analyzing and verifying tasks and data parallelism, the categorical approach

becomes much better approaching than other ones in theory of algebras. From an applicative aspect of the approach, moreover, formalizing tasks parallel and data parallel on BioChipNets is a categorical specification of middleware that can be used to develop implementations for core-to-core and agent-based networking.

Chapter 6 by L. Guang, J. Plosila, J. Isoaho, and H. Tenhunen presents a novel design approach, hierarchical agent-monitored SoC (HAMSoC), by elaborating its formal specification framework and demonstrating a design example of hierarchical power monitoring on NoCs. This approach provides scalability in terms of both design effort and physical overhead. The formal specification framework of HAMSoC enables efficient system-level specification and modeling for early-stage development. It adopts a highly abstracted formal language to specify exclusively the monitoring operations and parameters, with proper exposure of SW/HW interfaces. The FSM model is used for state transition analysis in monitoring operations. The specification is transformed into generic formal languages so that existing verification tools can be used for further system development.

Chapter 7 by L. Petre et al. discusses a middleware language based on formal methods that has been developed for real networks to be adapted to applications running on NoC. The chapter presents how to place modules that communicate often in each other's vicinity for efficiency. This becomes even more interesting if the NoC consists of vertically stacked layers, commonly referred to as 3-D NoCs. Furthermore, three dynamic alternatives for replacing an application are analyzed, some of which are centralized and others are distributed.

Finally, Chapter 8 by H. Zakaria, E. Yahya, and L. Fesquet discusses a survey on different problems facing designers over the nanometric era. Analyses and solutions to each of these challenges are presented that enable the design of a self-adaptable SoC. GALS systems are considered and some proposed solutions are also applicable to simpler designs.

3. Remarkable Features of the Book

This title is the third book in a series on Embedded Multi-Core Systems (EMS) published by CRC Press. The EMS series is under the editorial supervision of the Integrated Microsystems Research Group, which is one of the research groups of the Electrical and Computer Engineering Department (ECE), Faculty of Engineering at the University of Victoria (UVic) in Canada.

This book has the following remarkable features:

- Provides a comprehensive reference on ANoC

- Presents state-of-the-art techniques in ANoC
- Formally specifies, develops and verifies bio-inspired on-chip networks

- Includes illustrative figures facilitating easy reading

- Discusses emerging trends and open research problems in ANoC

The book serves as a comprehensive and essential reference on autonomic networking-on-chip and is intended as a textbook for senior undergraduate- and graduate-level courses. It can also be used as a supplementary textbook for undergraduate courses. The book is a useful resource for students and researchers to learn autonomic networking-on-chip. In addition, it will be valuable to professionals from both academia and industry and generally has instant appeal to people who would like to contribute to autonomic networking-on-chip technologies.

We highly hope you enjoy reading the book.

4. Reviews and Testimonials

"The FIRST Book to Assess Research Results, Opportunities, & Trends in BioChipNets".
– CRC Press

"The book has come into being from a fine collection of chapters emphasizing the multidisciplinary character of investigations from the point of view of not only the ANoC field involved but also the formal methods. The book, which is specially dedicated to reporting on recent progress made in the field of bio-inspired on-chip networks (BioChipNets), will usefully serve as a technical guide and reference material for engineers, scientists, practitioners, and researchers by providing them with state-of-the-art research results and future opportunities and trends. To the best of my knowledge, this is the first book that presents achievements and findings of ANoC research covering the full spectrum of formalizing BioChipNets. These make the book unique and, in more than one respect, a truly valuable source of information that may be considered a landmark in the progress of ANoC".

– Petre Dini, Advisory Committees Board Chair of IARIA

References

[1] P.C. Vinh(2011) *Autonomic Networking-on-Chip: Bio-Inspired Specification, Development, and Verification* (CRC Press), 1st ed.