

Efficient FPGA-based phase measurement for heterodyne interferometry

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Abstract

INTRODUCTION: Phase measurement plays an important role in high-precision applications such as optical interferometry, metrology, and scientific instrumentation, where accurate and low-latency phase information is required.

OBJECTIVES: This paper presents a real-time phase difference measurement system implemented on a low-cost Kintex-7 (XC7K325T) FPGA.

METHODS: The proposed system directly estimates the instantaneous phase difference between two heterodyne signals using a feed-forward quadrature processing approach. Each input signal is processed with filtering and the Hilbert transform to obtain the in-phase and quadrature components, followed by amplitude normalization to reduce the influence of variations in signal magnitude. The phase difference is then computed by quadrature mixing to generate sine and cosine components, which are converted to phase values using a CORDIC-based arctangent module. The entire signal processing chain is implemented in a fully pipelined FPGA architecture, enabling deterministic, low-latency real-time operation.

RESULTS: Experimental results using controlled heterodyne signals generated by a Moku: Lab instrument demonstrate that the proposed system provides accurate phase measurements with a small, consistent offset (approximately 1.2°) and an end-to-end processing latency of approximately 420 ns.

CONCLUSION: The proposed fully pipelined FPGA architecture is suitable for deterministic, low-latency real-time phase measurement in interferometric systems.

Keywords: Custom low-cost field-programmable gate array, high-speed analog-to-digital converter, vibration and displacement measurement

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1. Introduction

Phase measurement is a foundational technique in many high-precision domains such as optical metrology, vibration analysis, and displacement sensing. Among the available methods, heterodyne interferometry is particularly distinguished by its ability to resolve phase with exceptional precision [1–8]. By exploiting the interference of two coherent optical beams with a small frequency offset, heterodyne interferometry produces a

beat signal in which the phase information of interest is encoded, enabling highly sensitive and robust measurements.

Despite these advantages, the practical realization of heterodyne-based measurement systems presents several technical challenges, particularly in real-time signal processing, stringent accuracy requirements, and hardware efficiency. These challenges are further intensified in embedded measurement platforms, where power

consumption, computational capability, and deterministic timing must be carefully considered. Fully analog implementations can perform phase processing directly in hardware [9], but correcting additional hardware-induced errors may require dedicated calibration circuitry or hardware modification [10]. In contrast, reconfigurable digital implementations allow additional error-compensation functions to be incorporated through logic updates as required by the application [11]. Quasi-digital signals encode the measurand as parameters such as frequency, duty cycle, or phase [12], providing improved noise immunity [13] and potentially avoiding conventional analog-to-digital conversion (ADC) when such outputs are available directly [14]. However, their performance may still be affected by timing uncertainty [12] and resolution–bandwidth trade-offs [15]. In heterodyne interferometry, the photodetector produces an analog electrical beat signal that is digitized before subsequent phase estimation [11]. Therefore, resolving small displacement-induced phase variations requires both high-quality waveform acquisition and real-time processing with low and predictable latency.

In recent years, field-programmable gate arrays (FPGAs) have emerged as a promising platform for real-time phase measurement due to their inherent parallelism, reconfigurability, and deterministic timing behavior. Several FPGA-based phase measurement systems have been reported in the literature [11,16–18]. However, many existing solutions still exhibit limitations in processing latency, robustness to noise, or incomplete hardware integration, which restrict their applicability to high-speed and dynamically varying interferometric systems.

For example, Straube et al. [16] proposed an FPGA-based signal processing scheme for heterodyne interferometry that primarily focuses on frequency division and envelope detection, without providing a direct, fully hardware-based phase-estimation stage. Gerberding et al. [17] presented a high-precision phasemeter core for intersatellite interferometry. However, the proposed system relies heavily on extensive modeling and simulation, with critical components of the phase estimation pipeline implemented in software rather than as

fully synthesized hardware logic. Mitra and Nayak [18] developed a modular FPGA-based phase measurement system using zero-crossing and comparator techniques. At the same time, while hardware-efficient, this approach exhibits limited robustness to noise and potential phase ambiguity. Similarly, Vera-Salas et al. [11] introduced an FPGA-based smart sensor for industrial displacement measurement. Still, the system is primarily optimized for low-to-moderate-frequency signals and lacks the flexibility required for high-speed interferometric applications.

In this work, a fully hardware-integrated, feed-forward phase-difference measurement system combining high-speed waveform acquisition with real-time FPGA processing is presented. The proposed approach directly computes the instantaneous phase difference between two heterodyne signals using quadrature signal processing, without relying on iterative feedback or software-based computation. The complete signal processing chain (including synchronization, filtering, Hilbert transformation, amplitude normalization, and phase demodulation) is implemented using pipelined and parallel FPGA modules to ensure deterministic timing and ultra-low-latency operation.

The system is implemented on a Kintex-7 FPGA (XC7K325T) [19] in combination with a high-speed analog-to-digital conversion front-end (Texas Instruments AFE7225, 12-bit resolution, 100 MS/s sampling rate) [20], enabling real-time, point-by-point phase computation. Experimental results demonstrate that the proposed architecture achieves high phase measurement accuracy with low processing latency and efficient FPGA resource utilization, making it well-suited for high-speed interferometric measurement applications.

2. Methodology

2.1 Overview of the phase measurement system for interferometry



Figure 1. System overview

Fig. 1 illustrates the overall block diagram of the proposed FPGA-based phase measurement system. Two analog input signals (Input A and Input B), together with a

common clock signal, are acquired by a dual-channel ADC (AFE7225). The digitized data are transferred to the FPGA via an FPGA Mezzanine Card (FMC)-ADC adapter board

[21] using a low-voltage differential signaling (LVDS) interface. Inside the Kintex-7 FPGA (XC7K325T), a hardware synchronization module aligns and validates the incoming data before forwarding it to the phase meter core, which computes the phase difference between the two input signals.

The hardware synchronization module is responsible for clock alignment, frame synchronization, and data validation of the incoming LVDS streams, providing a stable and deterministic data interface for subsequent processing stages within the FPGA. Once synchronization is complete, the phase meter core computes the phase

difference between the two input signals (Input A and Input B). [22]

All functional blocks in the system, including hardware synchronization, bandpass filtering, Hilbert transformation, amplitude normalization, phase mixing, and integration, were implemented in Verilog hardware description language (VHDL) and synthesized using Xilinx Vivado for a Kintex-7 (XC7K325T) device. The phase meter core operates at 100 MHz, matching the ADC output data rate.

2.2 Operating Principle of the Phase Meter

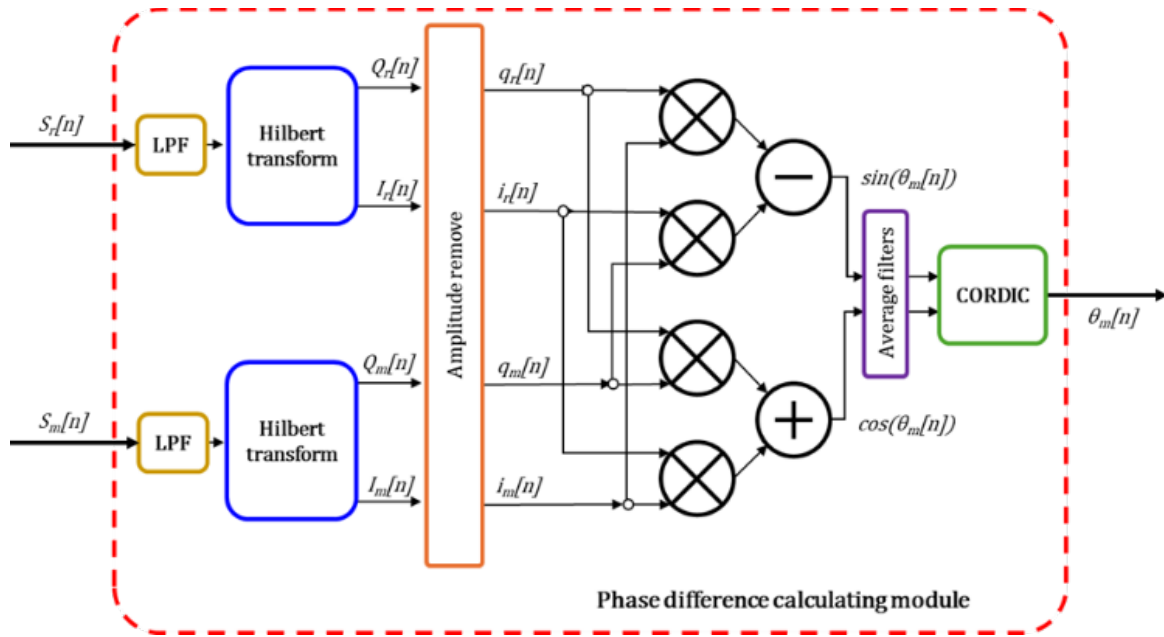


Figure 2. Phase meter architecture

Fig. 2 presents the architecture of the phase meter module. In this model, signals from Input A and Input B are assumed to be sinusoidal waveforms of equal frequency. Input A is treated as the reference signal (S_r), while Input B carries the measured signal (S_m), represented as

$$S_r = A_r \times \cos(\Delta\omega \times n), \quad (1)$$

$$S_m = A_m \times \cos(\Delta\omega \times n). \quad (2)$$

where, A_r and A_m denote the amplitudes, $\Delta\omega = 2\pi \times (f/fs)$ is the normalized angular frequency, n is the discrete time index, and θ_m represents the instantaneous phase shift between the two signals.

To suppress background noise and reduce distortion-induced errors, both input signals are passed through low-pass filters (LPFs). The filters were designed to isolate the heterodyne beat frequency component, ensuring accurate Hilbert transformation and phase demodulation. A finite impulse response (FIR) filter with a Kaiser window was

selected due to its adjustable trade-off between main-lobe width and side-lobe attenuation. The filter is designed with the parameters shown in Table 1.

Table 1. Design parameters of the FIR filter

Parameters	Value/Configuration
Filter type	FIR LPF (Kaiser window)
Order	128 taps
Cutoff frequencies	1.5 MHz
Sampling rate	100 MS/s

The coefficients were generated in MATLAB and loaded directly into the FPGA as constants. The passband ripple is less than 0.05 dB, and the stopband attenuation exceeds 60 dB, ensuring a high-fidelity phase signal.

$$I_r = A_{r1} \times \sin(\Delta\omega \times n), \quad (3)$$

$$Q_r = A_{r2} \times \cos(\Delta\omega \times n), \quad (4)$$

$$I_m = A_{m1} \times \sin(\Delta\omega \times \theta_m), \quad (5)$$

$$Q_m = A_{m2} \times \cos(\Delta\omega \times n + \theta_m). \quad (6)$$

The amplitude differences among the signals are eliminated by an amplitude-removal block, which transforms the signals into an amplitude-independent form by multiplying each signal by a corresponding scaling factor k . This coefficient is determined empirically through repeated experimental calibration. After passing through this block, the signals can be expressed as

$$i_r = \sin(\Delta\omega \times n), \quad (7)$$

$$q_r = \cos(\Delta\omega \times n), \quad (8)$$

$$i_m = \sin(\Delta\omega \times n + \theta_m), \quad (9)$$

$$q_m = \cos(\Delta\omega \times n + \theta_m). \quad (10)$$

Next, multipliers together with adder and subtractor blocks combine the four intermediate signals to generate the sine and cosine components of the phase difference, denoted as $\sin(\theta_m)$ and $\cos(\theta_m)$. These signals are smoothed using simple averaging filters before being processed by a coordinate rotation digital computer (CORDIC) block (implemented using a built-in Xilinx intellectual property (IP) core) to compute the phase θ_m via the arctangent operation [23].

3. Results

To evaluate the performance of the programmed phase meter, an experiment was set up as illustrated in Fig. 3.

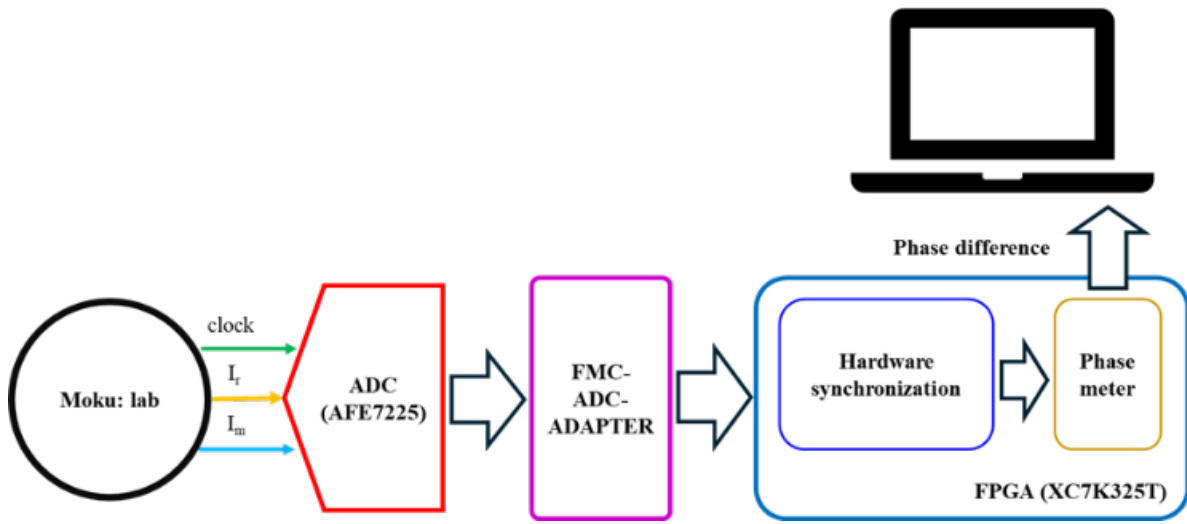


Figure 3. Experiment setup

Fig. 3 depicts the experimental configuration used to assess the phase meter designed according to the proposed method in this paper. In this setup, Moku: Lab [24] serves as the source providing three signals: clock, S_r and S_m . The measured phase results are transmitted directly to a laptop for monitoring, recording, and evaluation. The frequency and amplitude of the S_r and S_m signals are set to 1 MHz and 100 mV, respectively. A summary of key experimental parameters is provided in Table 2 below for clarity and reproducibility.

Table 2. Key experimental parameters of the proposed FPGA-based phase measurement system

Parameters	Value/Configuration
ADC sampling rate	100 MS/s
ADC resolution	12 bits
Input signal frequency	1 MHz

Input signal amplitude	100 mV
Phase offsets tested	0°, -7.2°, -25.2°, -50.4°
LPF design	FIR filter, 64 taps, 1.5 MHz passband
FPGA core frequency	100 MHz

These parameters were carefully selected to match the characteristics of the interferometric setup and to reflect typical operating conditions for real-time phase measurement. Meanwhile, the phase offset θ_m is adjusted sequentially to values of 0°, -7.2°, -25.2°, and -50.4°.

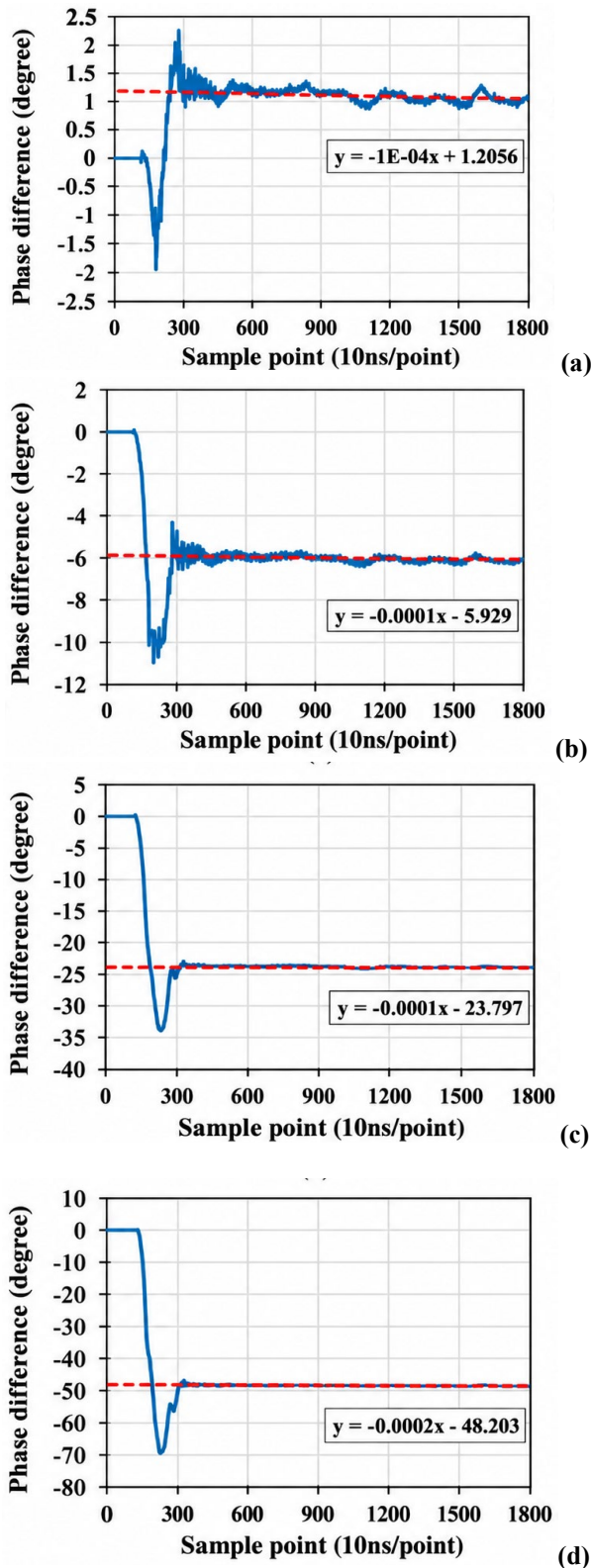


Figure 4. Recorded results of the calculated phase offset for each input case: (a) 0° , (b) -7.2° , (c) -25.2° , and (d) -48.2°

The dark blue line represents the measured phase signal over time, while the red line indicates the corresponding linear trendline, illustrating the system's stability and accuracy across varying phase shifts.

Fig. 4 shows the measured phase offsets under four input phase-shift conditions (0° , -7.2° , -25.2° , and -48.2°). At the beginning of each measurement, a short transient response is observed following the applied phase step, after which the measured phase signal settles to a steady value. This transient corresponds to the transition interval immediately after the phase offset is introduced. After this interval, the measured phase signals remain stable around their mean values, with only small fluctuations observed over time. The fitted regression lines exhibit slopes close to zero, indicating good temporal stability of the phase measurement.

For the 0° input condition, the measured phase offset is approximately 1.2° . For larger applied phase shifts, such as -25.2° and -50.4° , the measured steady-state values are -23.8° and -48.203° , respectively, which closely agree with the corresponding input phase offsets. These results confirm that the proposed system can accurately measure a wide range of phase differences.

To provide a quantitative evaluation of measurement accuracy, Table 3 summarizes the mean error and standard deviation of the measured phase offsets for each test case. The results indicate that the system maintains a consistently low error level across all evaluated phase conditions.

Table 3. Summary of phase measurement accuracy

Input Phase Offset ($^\circ$)	Measured Offset ($^\circ$)	Average error ($^\circ$)	Std. Deviation ($^\circ$)
0.0	1.2	+1.2	0.6
-7.2	-7.4	-0.2	0.8
-25.2	-23.8	+1.4	0.9
-50.4	-48.2	+2.2	1.0

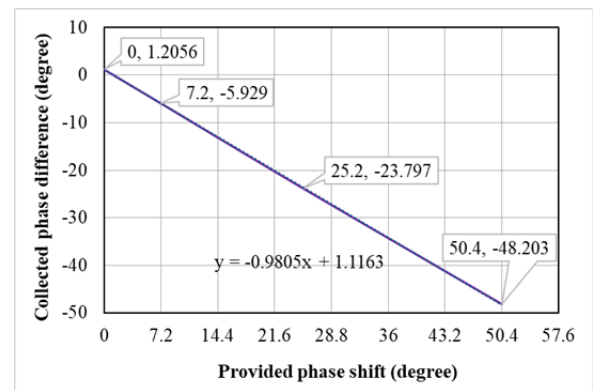


Figure 5. Correlation between the phase offset supplied by Moku: Lab and the phase offset

calculated by the proposed phase measurement system

Fig. 5 illustrates the linear correlation between the input phase offsets provided by the Moku: Lab device and the corresponding phase offsets obtained from the proposed measurement system. A linear regression fitted to the measured data yields a slope of -0.9805 and a small offset error with a y-intercept of 1.1163° , indicating a strong linear relationship between the applied and measured phase values across the tested range. These results confirm that the system can accurately reproduce the input phase offsets with good linearity, making it suitable for applications requiring precise phase measurement and monitoring.

The end-to-end processing latency of the phase measurement system was evaluated from ADC sampling to phase output. Based on post-implementation timing analysis and oscilloscope-based input-output delay measurements, the system exhibits a latency of approximately 420 ns, corresponding to 42 clock cycles at an operating frequency of 100 MHz. For the 1 MHz test signal used in this study, this latency corresponds to approximately 42% of one signal period. However, in the monitoring applications considered, the 1 MHz signal serves as a carrier, while the phase variation of interest typically occurs below 200 Hz. Therefore, the measured latency remains sufficiently small for real-time phase tracking. In addition, since both input channels are processed through the same synchronous pipeline and therefore experience the same processing latency, the delay does not directly affect the measured phase difference. This low, deterministic latency is achieved through a fully pipelined, parallel FPGA architecture. Compared with existing FPGA-based implementations reported in [16] and [18], which exhibit processing delays on the order of tens of microseconds, the proposed system offers a lower processing delay, making it suitable for real-time measurement and monitoring applications.

Although the experimental setup employed a Moku: Lab device as a relatively clean signal source, practical interferometric systems may be affected by noise, amplitude variations, and signal distortions. In the proposed system, the inclusion of bandpass filtering and amplitude normalization in the signal processing chain helps mitigate these effects and improves measurement stability under non-ideal input conditions. Experimental results obtained with degraded input signals (100 mV) indicate that the measured phase values remain stable within a limited error range, supporting the system's applicability in practical measurement environments. Further investigation of system performance under more severe noise conditions and the integration of advanced post-processing techniques are left for future work.

4. Conclusion

This paper presented a real-time FPGA-based phase-measurement system, combined with a high-speed ADC

module, for direct computation of the phase difference between two input signals. By employing a fully hardware-integrated signal-processing chain, the proposed implementation demonstrates that accurate, temporally stable phase measurement can be achieved with deterministic latency on an embedded FPGA platform.

Experimental results obtained with controlled input signals confirm that the proposed architecture reliably reproduces known phase offsets with good linearity and low steady-state error. The measured performance, together with the low processing latency enabled by the pipelined hardware design, verifies the practical feasibility of the proposed approach for real-time phase measurement applications.

While the current work focuses on validating the system architecture and its real-time performance, more comprehensive academic evaluations, such as deployment in a real interferometric setup, detailed signal-integrity analysis, and testing under more complex operating conditions, remain important directions for future research. These studies will further characterize the system behavior and extend the presented work toward broader interferometric measurement scenarios.

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