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Voltage Compensation-Type Current Limiter Based on Hybrid Distribution Transformer for Power Quality Enhancement

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Abstract

This paper presents a voltage compensation-type current limiter based on a hybrid distribution transformer (HDT) structure, which integrates a three-winding transformer, AC/DC converter, DC/AC converter, current-limiting unit, bypass switches, and a series transformer. The HDT operates under four distinct modes: steady-state operation, voltage recovery, active current limiting, and passive current limiting. The proposed system effectively compensates voltage sags and limits fault currents by dynamically switching between these modes. Simulation results demonstrate that the method can quickly restore load-side voltage during upstream voltage sags and efficiently limit fault currents during downstream faults. The proposed strategy ensures continuous and reliable operation of sensitive loads under fault conditions.

Keywords: Current limiting, Hybrid distribution transformer, Power quality, Voltage compensation

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1. Introduction

Power quality issues, including voltage sags, swells, flicker, harmonic distortion, voltage unbalance, and excessive fault currents, have become increasingly critical in modern distribution systems due to the rapid integration of renewable energy, electric vehicle charging, and nonlinear loads [1]. These disturbances can severely affect sensitive industrial processes, degrade equipment lifespan, and threaten the overall stability of the grid.

To mitigate voltage fluctuations, on-load tap changers (OLTCs) are widely used in conventional distribution transformers. However, OLTCs typically operate with discrete tap positions and slow mechanical switching (on the order of several seconds), making them incapable of providing fast, continuous voltage regulation in response to transient disturbances such as voltage sags or swells [2]. Additionally, traditional transformers lack intrinsic fault current limiting or harmonic suppression capabilities, which limits their ability to address comprehensive power quality challenges in real time[3].

To address these limitations, power electronic transformers (PETs), also known as solid-state transformers (SSTs), have been proposed. They integrate multi-stage converters and high-frequency isolation to achieve bidirectional, fast, and flexible power flow control [4]-[6]. Nevertheless, their practical application is constrained by high cost, relatively low efficiency, complex cooling requirements, and concerns about large-scale operational reliability[7].

As a practical compromise, the hybrid distribution transformer (HDT) combines the robustness of conventional transformers with the fast control capability of power electronic modules[8][9]. This hybrid configuration reduces cost and thermal stress while improving dynamic performance.

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In response to challenges such as voltage sags, swells, and three-phase unbalance, the hybrid distribution transformer (HDT) has been introduced as a promising compromise solution that combines the reliability of conventional transformers with the fast control capability of power electronic modules [10][11]. HDTs maintain the primary power path through a traditional low-frequency transformer while incorporating a parallel power electronic branch to perform dynamic voltage regulation and harmonic compensation. However, during severe overcurrent or short-circuit faults, excessive fault currents can damage transformer windings, stress power electronic components, and disrupt protection coordination. These issues underscore the importance of fault current limiting technologies to ensure system safety and reliability. Fault-current limiters (FCLs) have evolved rapidly to address rising short-circuit levels in modern networks. Recent work emphasizes hybrid and solid-state approaches that combine the speed of power-electronics with the steady-state robustness of passive elements. Self-powered solid-state FCLs harvest energy from the fault condition to drive switching devices, reducing auxiliary supply needs while achieving sub-millisecond limitation[12]. Hybrid FCLs—often pairing superconducting or saturable-core elements with semiconductor switches—offer fast initial limiting and sustained impedance without excessive use of HTS material[13][14]. For DC systems and traction networks, arcless hybrid FCL/circuit-breaker concepts enable soft interruption and reduced mechanical stress[15]. Practical designs also include optimized self-driving rheostats and commutation circuits to balance loss, cost, and interruption capability[16]. Overall, recent studies demonstrate scalable FCL solutions suitable for VSC-HVDC, distribution grids, and rail systems, with active research focused on reliability, recovery time, and cost reduction.

In this paper, we propose a voltage compensation-type current limiter based on the HDT for power quality enhancement. This method can simultaneously achieve voltage sag mitigation through fast voltage compensation and fault current limitation via coordinated control of the power electronic auxiliary path. The proposed approach provides an efficient and practical solution to enhance power quality in modern distribution systems.

2. Topology

As shown in Figure 1, the three-winding transformer, together with the AC/DC converter, DC/AC converter, current-limiting unit, bypass switches and the series transformer, constitutes the HDT. Winding 1 of the three-winding transformer is connected to the 10kV medium-voltage side of the power grid, while winding 2 is connected to the 220V low-voltage load side, winding 3 is connected to the AC side of the AC/DC converter. The DC side of the AC/DC converter is connected to the DC side of the DC/AC converter through a capacitor C and the current-limiting unit. The rectifier provides a stable voltage for the DC side of the inverter and supplies power to the inverter. The inverter achieves voltage support and current limiting functions by applying voltage to the series transformer.

The current-limiting unit[17] consists of a current-limiting impedance (comprising R_{limit} and X_{limit}, two anti-parallel thyristors, a bypass switch and a diode). In the non-passive current-limiting modes (voltage recovery mode and active current-limiting mode), both the anti-parallel thyristors are turned on and the switch is off, thereby bypassing the current-limiting unit. In the passive current-limiting mode, both the anti-parallel thyristors are turned off and the switch is on, the DC/AC converter is blocked, and the current-limiting unit is enabled.

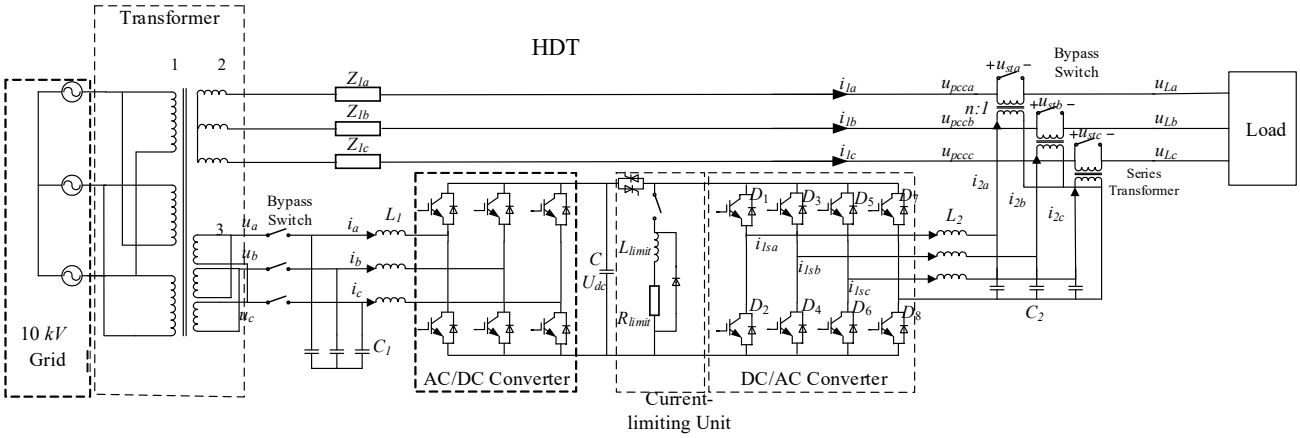


Figure 1. Topological structure of HDT

2.1. Control strategy of the AC/DC converter

As shown in Figure 2, the AC/DC converter consists of a two-level converter, whose AC side is connected to the auxiliary windings of the multi-winding transformer; the DC side of the converter is also connected to the DC bus. U_{dc} denotes the

DC-side voltage; u_{a1}, u_{b1}, and u_{c1} are the three-phase voltages on the converter switch side respectively; L_1 is the filter inductor of the converter; i_a, i_b, and i_c are the three-phase currents on the AC side of the converter; u_a, u_b, and u_c are the output voltages of the auxiliary windings of the multi-winding transformer. For the convenience of analysis, the following assumptions are made: the filter inductance parameters of each phase are the same, and the losses of switching devices, line resistance, and parasitic resistance of inductors are neglected.

The AC side of the converter is connected to a three-phase balanced power grid with no unbalanced current. Since we regard the switches of each phase as ideal switches, the state of the circuit can be represented by switching functions. Let the switching functions of phases A, B, and C be S_A, S_B, and S_C respectively. When the upper switch turns on and lower switch turns off, the value of $S_{A,B,C}$ is 1; otherwise, the value of $S_{A,B,C}$ is 0. According to the principles of KCL and KVL, we can derive its mathematical model of Figure 2 as follows:

$$\begin{cases} S_{A,B,C}U_{dc} - L_1\dfrac{di_{a,b,c}}{dt} = u_{a,b,c} + u_{no} \\ C_1\dfrac{du_{c1}}{dt} = S_A i_a + S_B i_b + S_C i_c \end{cases} \tag{1}$$

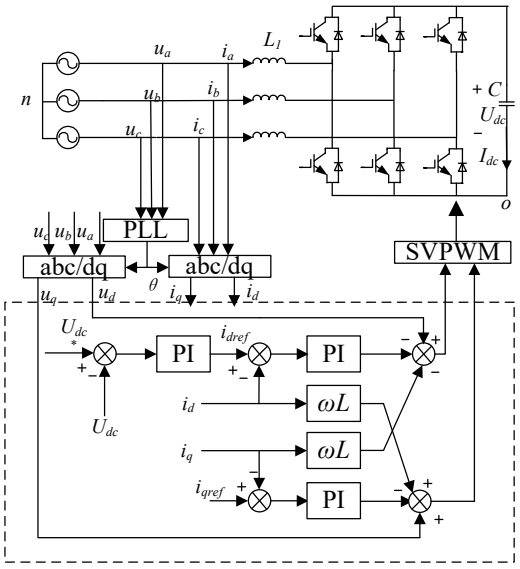


Figure 2. Control block diagram of the AC/DC converter

For a three-phase three-wire symmetric power grid, the following relationship exists between the grid-side voltage and current:

$$\begin{cases} i_a + i_b + i_c = 0 \\ u_a + u_b + u_c = 0 \end{cases} \tag{2}$$

Through equations (1) and(2), we can derive:

$$u_{no} = \frac{1}{3}(S_A + S_B + S_C)U_{dc} \tag{3}$$

In the stationary three-phase coordinate system, the three-phase power supplies are mutually coupled. If the coordinate transformation method of the two-phase rotating coordinate system is adopted, and the grid input voltage is balanced, the d and q components will both be DC at this time. In the dq coordinate system, the d-axis current is the system input active current, and the q-axis current is the system input reactive current. In this way, the decoupled and independent control of the active and reactive components on the three-phase grid side can be realized. Therefore, the design of the regulator is convenient, the calculation is simple, and it is easy to achieve an input power factor of 1. Thus, for the mathematical model under the dq coordinate system, the most commonly used controller in the design of the current loop controller is the proportional-integral controller.

According to Equation(1), when we convert the mathematical model of the converter in the abc three-phase stationary coordinate system to the two-phase rotating dq coordinate system, the mathematical model of the dq axes shown in Equation (4) can be obtained.

$$\begin{cases} L_1\dfrac{di_d}{dt} = u_{d1} - u_d + \omega L_1 i_q \\ L_1\dfrac{di_q}{dt} = u_{q1} - u_q - \omega L_1 i_d \end{cases} \tag{4}$$

Among them, ω is the angular frequency of the Synchronous Reference Frame (SRF), u_{d1} and u_{q1} are the output voltages of the converter in the dq two-phase rotating coordinate system.

Let $u_{d1} = u_d - \omega L_1 i_q + \dfrac{k_p s + k_i}{s}\left(i_d^* - i_d\right)$ and $u_{q1} = u_q + \omega L_1 i_d + \dfrac{k_p s + k_i}{s}\left(i_q^* - i_q\right)$, then we can obtain:

$$\begin{cases} L_1 s i_d = \dfrac{k_p s + k_i}{s}\left(i_d^* - i_d\right) \\ L_1 s i_q = \dfrac{k_p s + k_i}{s}\left(i_q^* - i_q\right) \end{cases} \tag{5}$$

With reasonable parameter settings, the current loop can be approximated as a small inertia link.

As for the voltage loop, according to the low-frequency model of the three-phase two-level rectifier , when the switching frequency is much higher than the fundamental frequency of the grid, the harmonic components in PWM can be neglected. At this time, the switching functions $S_{A,B,C}$ can be expressed as:

$$\begin{cases} S_A \approx 0.5m\cos(\omega t-\theta)+0.5 \\ S_B \approx 0.5m\cos(\omega t-\theta-120^\circ)+0.5 \\ S_C \approx 0.5m\cos(\omega t-\theta+120^\circ)+0.5 \end{cases} \quad (6)$$

Where m is the PWM modulation index; θ is the initial phase angle of the fundamental wave of the switching function. For unit power factor sinusoidal current control, the grid-side currents of the three-phase two-level rectifier are:

$$\begin{cases} i_a \approx I_m \cos\omega t \\ i_b \approx I_m \cos(\omega t-120^\circ) \\ i_c \approx I_m \cos(\omega t+120^\circ) \end{cases} \quad (7)$$

By synthesizing equation. (1),(6) and(7), the DC-side current I_{dc} can be approximately expressed as:

$$I_{dc} \approx 0.75m\cos\theta I_m \quad (8)$$

Where $0.75m\cos\theta$ is a time-varying coefficient. For the convenience of control parameter design, the maximum value of this coefficient, 0.75 (since $m\leq 1$), can be used to replace this coefficient.

For the control structure shown in Figure 2, when a PI controller is used to control the DC-side voltage, the transfer function of the current loop can be approximated as a small inertia link, i.e.:

$$G_U(s)=\frac{K_u(1+T_u s)}{T_u s}, \quad G_I(s)=\frac{1}{3T_S s+1} \quad (9)$$

Where $G_U(s)$ is the DC-side voltage controller; $G_I(s)$ is the equivalent transfer function of the current closed loop; K_u and T_u are the parameters of the voltage controller; T_S is the sampling period. At this time, the open-loop transfer function of the voltage outer loop is:

$$W_{ou}(s)=\frac{0.75K_u(1+T_u s)}{CT_u s^2(3T_S s+1)} \quad (10)$$

According to equation (10), the parameters of the voltage outer loop controller can be designed.

2.2. Control strategy of the DC/AC converter

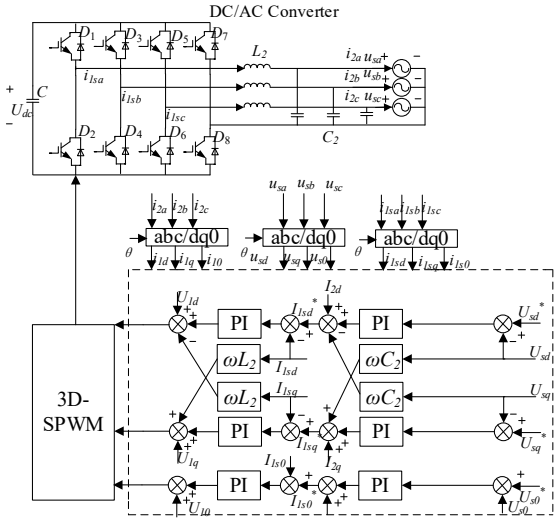


Figure 3. Control block diagram of the DC/AC converter

As shown in Figure 3, the AC/DC converter consists of a Two-Level Four-Leg Converter, whose AC side is connected in series in the main circuit; the DC side of the converter is connected to the DC bus.; u_{sa}, u_{sb}, and u_{sc} are the series Compensation voltages respectively; L_2 is the filter inductor; i_{2a} , i_{2b} , and i_{2c} are the series Compensation currents; i_{lsa} , i_{lsb} , and i_{lsc} are the inductor currents. Owing to its four-leg configuration, the converter enables enhanced control over zero-sequence voltage and current; accordingly, the dq-axis model expressions of the four-leg converter are given as follows:

$$\begin{cases} L_2\dfrac{di_{lsd}}{dt}=u_{outd}-u_{sd}+\omega L_2 i_{lsq} \\ L_2\dfrac{di_{lsq}}{dt}=u_{outq}-u_{sq}-\omega L_2 i_{lsd} \\ L_2\dfrac{di_{ls0}}{dt}=u_{out0}-u_{s0} \end{cases} \quad (11)$$

$$\begin{cases} C_2\dfrac{du_{sd}}{dt}=i_{lsd}-i_{2d}+\omega C_2 u_{sq} \\ C_2\dfrac{du_{sq}}{dt}=i_{lsq}-i_{2q}-\omega C_2 u_{sd} \\ C_2\dfrac{du_{s0}}{dt}=i_{ls0}-i_{20} \end{cases} \quad (12)$$

Among them, u_{out} denotes the output voltage of the converter. Based on the derivation results of equation (11) and (12), the control block diagram as shown in Figure 3 can be obtained.

3. Working Principle of Hdt

The working modes are divided into steady-state operation mode, voltage recovery mode, active current limiting mode, and passive current limiting mode, as described below.

3.1. Fault Detection

To quickly detect the occurrence of faults, it is necessary to obtain the phase and amplitude of voltage and current, which can be achieved through the virtual voltage/current method. Taking phase A current i_a as an example, the specific operation steps are as follows: Assume i_a=Isinωt, where I is the amplitude of phase A current, ω is the angular frequency, and t is time. Taking the derivative of i_a , we obtain:

$$i_a'(t) = \omega I \cos \omega t \tag{13}$$

The expression for symmetrical three-phase currents is:

$$\begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} = \begin{bmatrix} I \sin \omega t \\ I \sin(\omega t - \frac{2\pi}{3}) \\ I \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix} \tag{14}$$

Where I_b and I_c denote the virtual phase B current and virtual phase C current in the symmetrical three-phase currents, respectively.

Based on equation (13) and (14), the virtual phase B current is derived as:

$$I_b = -\frac{1}{2} I \sin \omega t - \frac{\sqrt{3}}{2} I \cos \omega t = -\frac{1}{2} I_a - \frac{\sqrt{3}}{2\omega} I_a' \tag{15}$$

After obtaining the values of phase A and phase B currents, the virtual phase C current is determined according to mathematical relationships:

$$I_c = -I_a - I_b = -\frac{1}{2} I_a + \frac{\sqrt{3}}{2\omega} I_a' \tag{16}$$

Narrowband band-pass filtering is performed on the fault current $i_{af}(t)$ to extract its fundamental component. This fundamental component is then used as the reference current signal to transform the virtual three-phase currents, as shown in the following equation:

$$\begin{bmatrix} I_{df} \\ I_{qf} \\ I_{0f} \end{bmatrix} = C \begin{bmatrix} \sqrt{2} I_f \sin(\omega t + \alpha_f) \\ \sqrt{2} I_f \sin(\omega t + \alpha_f - 120^\circ) \\ \sqrt{2} I_f \sin(\omega t + \alpha_f + 120^\circ) \end{bmatrix} = \begin{bmatrix} \sqrt{3} I_f \cos \alpha_f \\ -\sqrt{3} I_f \sin \alpha_f \\ 0 \end{bmatrix} \tag{17}$$

Since I_{df} and I_{qf} are known quantities obtained through actual measurement and calculation, the fundamental amplitude and phase jump of the short-circuit current are derived as equation.(18). The sudden change in the fundamental amplitude is taken as the main criterion for identifying a short-circuit fault. Threshold value I_{T1} and I_{T2} are set: if the measured fundamental amplitude is greater than I_{T1} or lower than I_{T2}, a fault is determined; otherwise, the system is considered to be in normal operation.

$$\begin{cases} I_f = \dfrac{\sqrt{3}}{3} \sqrt{I_{df}^2 + I_{qf}^2} \\ \alpha_f = \sin^{-1}\left(-\dfrac{I_{qf}}{\sqrt{I_{df}^2 + I_{qf}^2}} \right) \end{cases} \tag{18}$$

3.2. Steady-State Operation Mode

Before any fault occurs, the primary winding of the series transformer is short-circuited via the bypass switch, therefore ensuring the continuous and stable operation of the main circuit. The equivalent single-phase schematic diagram of the main circuit under this condition is shown in Figure 4 In this case, the load-side voltage is given by:

$$\dot{U}_L = \dot{U}_s - Z_1 \cdot \dot{I}_1 \tag{19}$$

where U_L is the load-side voltage, Us is the equivalent AC voltage source on winding 2 of the three-winding transformer, Z_1 is the line impedance, Z_2 is the load impedance and I_1 is the line current .

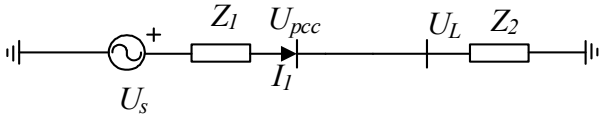


Figure 4. The equivalent single-phase schematic diagram

3.3. Voltage Recovery Mode

When the amplitude and phase of the voltage at the PCC are detected to change and exceed the threshold, a fault is considered to have occurred. Based on the detected load-side voltage U_L and current I_f, the load impedance is calculated as:

$$Z_f = \frac{\dot{U}_L}{\dot{I}_f} \tag{20}$$

The obtained load impedance is then compared with the pre-fault impedance Z_2. If the magnitude and phase angle of the impedance change, the fault is considered to occur on the

downstream load side; otherwise, it is considered to occur upstream. The judgment of the impedance depends on the specific circumstances, and here it is assumed that the load impedance remains unchanged. If the power factor remains constant, only the impedance angle needs to be judged.

When a fault is determined to be upstream (generally a voltage sag event, used as an example here), the system enters voltage recovery mode. The four-leg DC/AC converter is controlled via three-dimensional space vector pulse width modulation (3D-SVPWM) to generate a compensating voltage U_{st} on the series transformer, protecting the load and restoring the load-side voltage to its pre-fault level. The series transformer can be considered a voltage source; the equivalent single-phase schematic diagram of the main circuit under this condition is shown in Figure 5

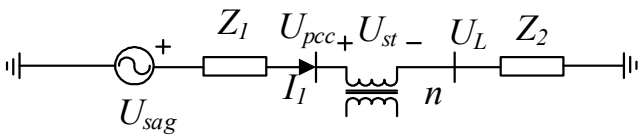


Figure 5. Equivalent circuit during voltage sag

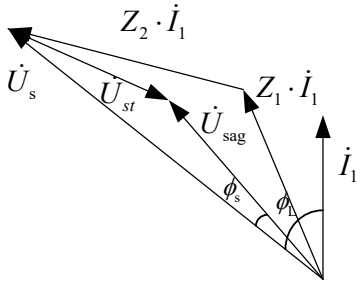


Figure 6. Vector diagram during voltage sag

The voltage sag event can be modeled as the source voltage becoming U_{sag}. Without series voltage compensation, the circuit equation becomes[18]:

$$\dot{U}_L' = \dot{U}_{sag} - Z_1 \cdot \dot{I}_1' \tag{21}$$

where $\dot{U}_L'$ is the load-side voltage after the voltage sag, $\dot{I}_1'$ is the line current after the voltage sag. For sensitive loads, which have high requirements for power quality, it is necessary to minimize fluctuations in the amplitude and phase of the load voltage after voltage fluctuations occur upstream. Since complete voltage compensation can restore the voltage amplitude and phase to the level before the voltage sag, adopting a complete voltage compensation strategy is quite feasible. The vector diagram under the complete voltage compensation strategy is shown in Figure 6. It can be seen that when adopting complete voltage compensation, the amplitude and phase angle of the compensation voltage output by the series transformer are respectively:

$$\begin{aligned} U_{st} &= \sqrt{U_s^2 + U_{sag}^2 - 2U_s U_{sag}\cos\phi_s} \\ \phi_{st} &= \arccos\left(\frac{U_{st}^2 + U_s^2 - U_{sag}^2}{2U_{st}U_s}\right) - \pi \end{aligned} \tag{22}$$

ϕ_s is the angle between U_s and U_{sag}, ϕ_{st} is the angle between U_s and U_{st}. The output active power is:

$$P_{st} = \left[U_{sag}\cos(\phi_L - \phi_s) - U_s\cos\phi_L\right] I_1 \tag{23}$$

ϕ_L is the angle between U_s and I_1.

When $U_s\cos\phi_L > U_{sag}\cos(\phi_L - \phi_s)$, $P_{st}<0$, and the series transformer injects active power into the power system; when $U_s\cos\phi_L < U_{sag}\cos(\phi_L - \phi_s)$, $P_{st}>0$, and the system instead injects active power into the series transformer.

3.4. Active Current Limiting Mode

When the fault is determined to occur downstream, the fault current limiting mode is entered, and the default is the active current limiting mode. To limit the current, the series transformer will generate an electromotive force to absorb power, thereby reducing the current in the line. The four-leg DC/AC converter is controlled via 3D-SVPWM to cause the primary side of the series transformer to produce a voltage, the compensating voltage $U_{st}=U_{pcc}-U_L'$, where U_{pcc} is the voltage of the PCC and U_L' is the post-fault load voltage, restoring the PCC voltage to its pre-fault value and limiting the current to the pre-fault level. A simple power system model shown in Figure 7 is used to explain the principle of the series compensator's fault current limiting method. In this model, Z is the impedance between the PCC and the node f where the fault occurs. The pre-fault voltage at point f is U_f. Under pre-fault conditions, the relationship between line current and voltage can be expressed as:

$$\begin{aligned} \dot{U}_s - \dot{U}_{pcc} - Z_1 \cdot \dot{I}_1 &= 0 \\ \dot{U}_{pcc} - \dot{U}_f - Z \cdot \dot{I}_1 &= 0 \end{aligned} \tag{24}$$

Typically, the line impedance is much smaller than the load impedance, so the voltage drop across the line is small compared to the load voltage. Most of the voltage and power are concentrated on the load, and the power consumed by the line can be neglected.

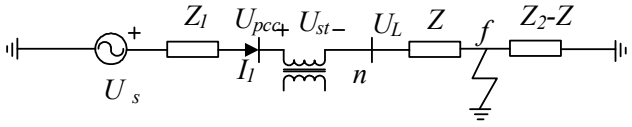


Figure 7. Equivalent circuit during short-circuit fault

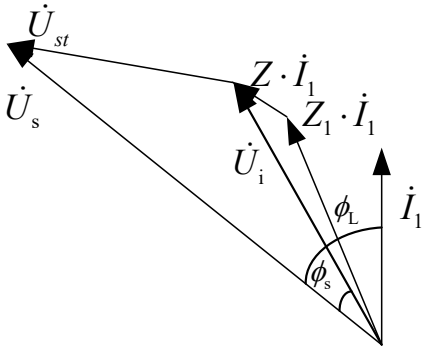


Figure 8. Vector diagram during short-circuit fault

When a downstream fault occurs at f, $U_f = 0$. Once the fault is detected, the series compensator injects a voltage U_{st} via the series transformer. U_{st} will reach a value that restores the PCC voltage to the same magnitude and vector as before the fault. This restoration is achieved by continuously adjusting U_{st}. When the current tends to stabilize, the output voltage u_{st} of the series transformer will be consistent with the pre-fault voltage u_{fpre} at the fault point. However, the fault location is random, making it difficult to quickly locate the fault occurrence position; thus, u_{fpre} is unknown. To address this, a continuous voltage injection method can be adopted to restore the voltage at the PCC point, thereby recovering the current. Specifically, the output voltage of the series transformer is controlled as $u_{st} = u_{pccp} - u_L$, where u_{pccp} is the pre-fault voltage at the PCC point, and u_L is the voltage on the load side during the current limiting process. Although the continuous variation of u_{st} will induce changes in u_L, u_{st} will continuously track the value of u_{pccp} . Consequently, the voltage at the PCC point will gradually approach u_{pccp} and eventually revert to u_{pccp}. At this stage, the line current will also recover to the pre-fault level, and the system enters a stable state. The relationship between line current and voltage during this phase can be expressed as:

$$\begin{aligned} \dot{U}_s - \dot{U}_{pcc} - Z_1 \cdot \dot{I}_1 = 0 \\ \dot{U}_{pcc} - \dot{U}_{st} - Z \cdot \dot{I}_1 = 0 \end{aligned} \tag{25}$$

The vector diagram of voltage and current at this point is shown in Figure 8 When the injected voltage U_{st} equals the pre-fault voltage U_f at the fault location, the fault current I_f is limited to the pre-fault load current I_1.

3.5. Passive Current Limiting Mode

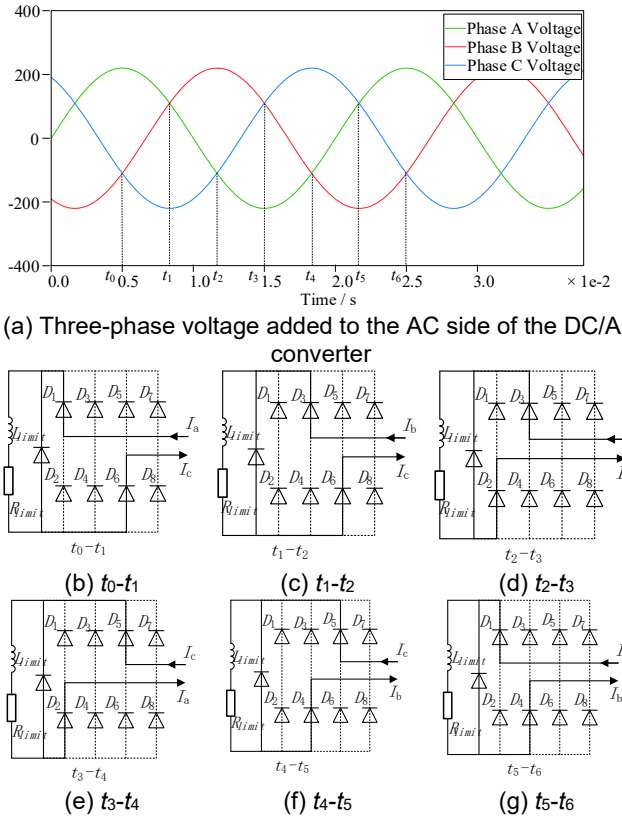


Figure 9. Schematic diagram of passive current limiting

After entering active current limiting mode, if the current flowing through the power electronic switches on the DC/AC side exceeds the threshold, upon detection, the system enters passive current limiting mode. The conduction condition for a three-phase grounded short circuit is shown in Figure 9. During the current limiting process, the conduction state of diodes D_1-D_6 is determined by the voltage across them: the diode with the highest anode voltage conducts among the common-cathode diodes, and the diode with the lowest cathode voltage conducts among the common-anode diodes. As shown in Figure 9(a), during the period t_0-t_1, phase C voltage is the lowest and phase A voltage is the highest, so D1 and D6 conduct. During t_1-t_2, phase B voltage is the highest and phase C voltage is the lowest, so D3 and D6 conduct (subsequent commutation follows this pattern). The conduction states are shown in Figure 9(b) to (g). For asymmetric short-circuit faults, the bypass switch of the non-faulted phase operates, continuing to supply power to the load. The faulted phase currents (phases B and C) are limited via the current limiting branch (R_{limit} and X_{limit}). The current conduction situation is similar to that during a three-phase short circuit and is not detailed here.

4. Results

In this section, a simulation model of the voltage compensation-type current limiter based on a hybrid

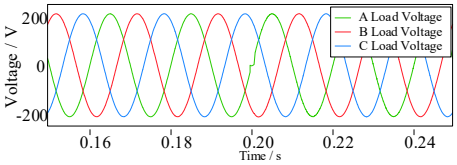
distribution transformer as shown in Figure 1 was built. The line parameters are shown in the following table 1.

Table 1. Line parameters

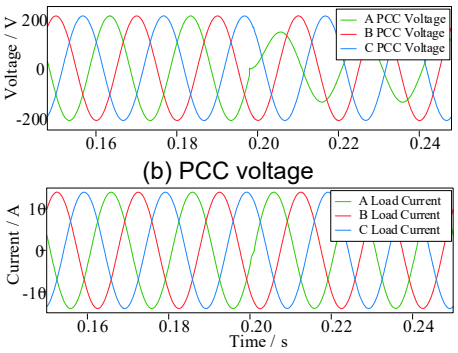
Parameter Name	Value	Unit
Z_1	0.19+2.16j	Impedance (Ω)
Z_2	15+2j	Impedance (Ω)
f	50	Frequency (Hz)
n	1	Turns Ratio
C	2000	Capacitance (μF)
L_2	6	Inductance (mH)
C_2	30	Capacitance (μF)

A voltage sag event is set to occur at t=0.2s, and the simulation results are shown in Figure 10 As can be seen from the figures, the voltage of Phase A sags and its phase changes at 0.2s. During this period, After 1ms, the fault detection unit detects and identifies the occurrence of a voltage sag, the series transformer is activated and compensates for the load voltage, and the load voltage quickly recovers to its pre-fault level, and the load-side current hardly changes. Therefore, the method proposed in this invention can effectively ensure the operation of sensitive loads.

Figure 11 shows the curves of load voltage, PCC voltage, and line current when a grounding short circuit occurs in phase A. It can be seen from the figures that at 0.2s, a grounding short circuit occurs in phase A, where only part of the load is short-circuited. At this time, the fault is not very severe, and the secondary-side current does not exceed the threshold, so it operates in the active current limiting mode. The PCC voltage is completely restored, since the current in the line has inertia, after the voltage at the PCC point is restored, the fault current still takes some time to recover to its pre-fault level. Nevertheless, after the series transformer is activated, the line current has already been limited. When the secondary-side current exceeds the threshold, as shown in Figure 12, the phase A load is completely short-circuited. Without limitation, the line current exceeds 150 A, far exceeding the pre-fault 14 A, which would cause great harm to the line. After adding the passive current limiting part, the phase A current is limited within 40 A. Before the fault is cleared, the phase A current does not cause damage due to being too large, and phases B and C are not faulty or affected, maintaining normal operation, which verifies the effectiveness of the proposed strategy.



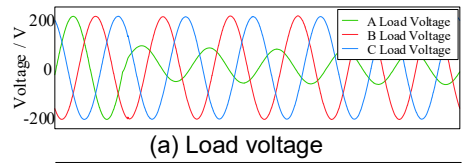
(a) Load voltage



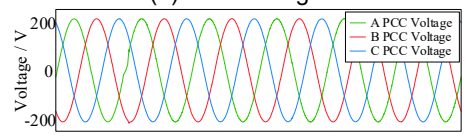
(b) PCC voltage

(c) Load current

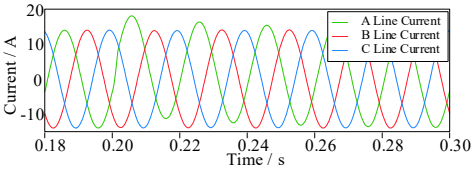
Figure 10. Voltage and Current during voltage sag



(a) Load voltage

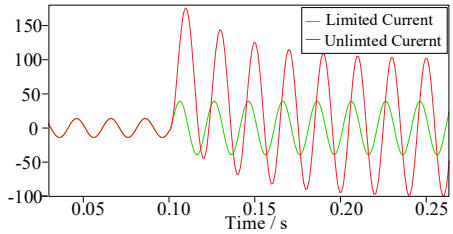


(b) PCC voltage

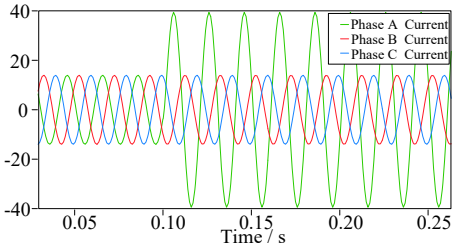


(c) Line current

Figure 11. Voltage and Current during short-circuit fault



(a) Limited current and unlimited current



(b) Limited three-phase current

Figure 12. Current under passive current limiting mode

5. HIL Experiments

To verify the effectiveness of the voltage recovery/current limiting strategy, this paper conducts Hardware-in-Loop (HIL) experiments based on the RTbox platform. The PLECS RTbox HIL simulator, developed by Plexim, is specifically designed for power electronics applications. It is equipped with abundant digital and analog interfaces, as well as an FPGA-integrated computing module. Its analog input channels can be used to receive analog signals from current and voltage sensors, while the digital output channels can generate PWM waves for driving power semiconductors. The simulator can simultaneously implement rapid simulation prototyping and HIL testing functions.

The HIL experimental platform based on RTbox3 is illustrated in Figure 13. In this experiment, the HDT is configured as a hardware circuit in RTbox1, which also operates in the rapid simulation prototype mode. PWM waves are output through the digital output channels to serve as the controller, and DB37 connection cables are used to realize the transmission of analog and digital signals.

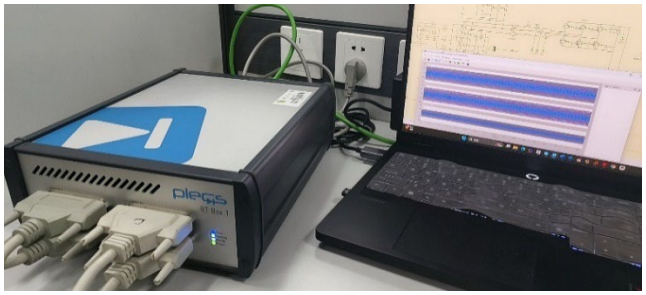
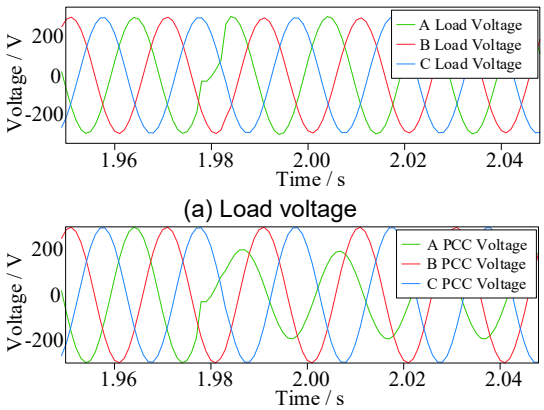


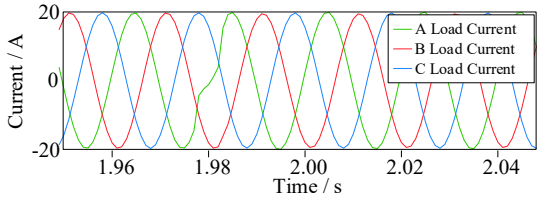
Figure 13. HIL Experimental Platform

During the simulation, upstream voltage sag faults and downstream load short-circuit faults of different degrees are set respectively. For the upstream voltage sag fault, the PCC point is grounded through a 2 Ω resistor. For the short-circuit faults, two scenarios are configured: the load-side 10 Ω resistor is grounded, and the entire load side is fully grounded.



(a) Load voltage

(b) PCC voltage

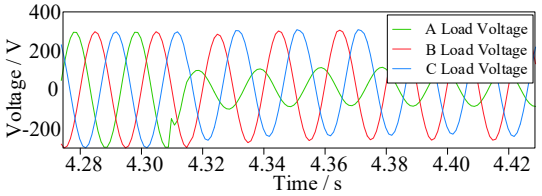


(c) Load current

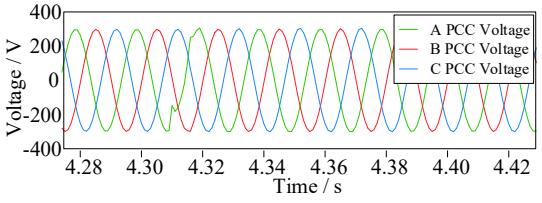
Figure 14. HIL Experimental diagram of voltage recovery mode

(1)Voltage recovery mode

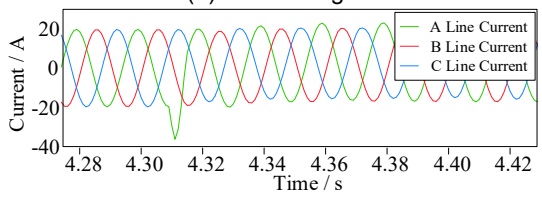
When a voltage sag fault occurs, the system detects the fault within a very short period of time and then enters the voltage recovery mode. As shown in Figure 14, the system experiences the fault between 1.97 s and 1.98 s. Subsequently, the load-side voltage quickly recovers to the pre-fault level, and the load-side current also rapidly restores, thereby ensuring the normal operation of sensitive loads.



(a) Load voltage



(b) PCC voltage



(c) Line current

Figure 15. HIL Experimental diagram of active current limiting mode

(2) Active current limiting mode

When the load is not fully grounded and the current does not exceed the threshold value, the HDT enters the active current limiting mode after fault detection, as shown in Figure 15. When the fault current is approaching -40 A, the series transformer of the HDT applies an electromotive force to limit the fault current. It can be seen from the figure that the limited current is not completely the same as the pre-fault current. This is because the impedance of the line is very

small, so a small voltage deviation at the point of PCC will cause a large change in current. Nevertheless, the function of the fault current limiter is to limit the current level, and it needs to be coordinated with other protection measures.

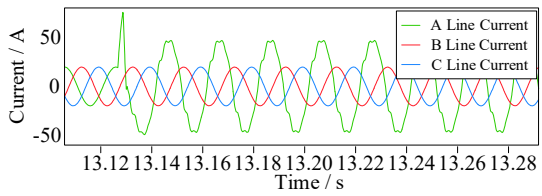


Figure 16. HIL Experimental diagram of passive current limiting mode

(3) Passive current limiting mode

When the load is fully short-circuited, the current becomes excessively large. To protect the power electronic devices of the hybrid distribution transformer (HDT), the system enters the passive current limiting mode. The line current after the load is fully short-circuited and current-limited is shown in Figure 16. The above experiments verify the effectiveness of the method proposed in this paper.

6. Conclusion

This paper proposes a voltage compensation-type current limiter based on a hybrid distribution transformer, which effectively integrates voltage support and fault current limiting functions within a single system. By coordinating the operation of the AC/DC converter, DC/AC converter, current-limiting unit, and series transformer, the HDT can flexibly switch among four working modes: steady-state operation, voltage recovery, active current limiting, and passive current limiting.

Simulation and experiment results demonstrate that the proposed method can quickly restore load-side voltage during upstream voltage sag events, ensuring stable operation of sensitive loads. In the case of downstream faults, the system can limit fault currents to the pre-fault level through active current limiting, and when necessary, further suppress excessive fault currents via the passive current-limiting mode. This dual-mode current-limiting strategy enhances system protection, reduces the risk of equipment damage, and improves fault ride-through capability. However, the method proposed in this paper relies on the rapidity and accuracy of fault detection. If the detection speed is too slow, the current may reach an excessively large value before current limiting is initiated, which could cause damage to the lines and loads. If the detection is overly sensitive, fluctuations in current and voltage may lead to maloperations. This is an aspect that can be improved in future research.

Overall, the proposed approach provides an effective and practical solution for improving power quality and ensuring the reliability of distribution networks under fault conditions. Future work will focus on further experimental validation and optimization of control strategies to enhance system performance.

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