EAI Endorsed Transactions
on Energy Web
Research Article EAI.EU

Design and Comparison of SEU Tolerant 10T Memory Cell for Radiation Environment Applications

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Abstract

Single event upsets (SEUs), which are caused by radiation particles, have emerged as a significant concern in aircraft applications. Soft mistakes, which manifest as corruption of data in memory chips and circuit faults, are mostly produced by SEUs. The utilization of SEUs can have both advantageous and detrimental effects in some critical memory applications. Nevertheless, in adherence to design principles, Radiation-Hardening-By-Design (RHBD) methodologies have been employed to mitigate the impact of soft mistakes in memory. This study presents a novel memory cell design, referred to as a Robust 10T memory cell, which aims to improve dependability in the context of aerospace radiation environments. The proposed design has several advantages, including reduced area, low power consumption, good stability, and a decreased number of transistors. Simulations were conducted using the TSMC 65nm CMO technology, employing the Tanner tool. The parameters of the RHB 10T cell were measured and afterwards compared to those of the 12T memory cell. The findings obtained from the simulation demonstrate that the performance of the 10T memory cell surpasses that of the 12T memory cell.

Keywords: Single Event Upset , Memory Chip, CMOS, 10T Memory cell

Received on 15 November 2023, accepted on 23 January 2024, published on 01 February 2024

doi: 10.4108/ew.5006

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1. Introduction

Memory applications in digital circuits are complicated by SEU. Soft mistakes must be reduced to preserve radiation-sensitive memories. Radiation particles cause SEU, which corrupts memory chips and permanently damages circuits, causing electronic system failure. Radiation-Hardening-By-Design approaches accommodate soft memory errors. RHBD uses commercial Complementary Metal-Oxide-Semiconductor foundry processes without any process or design changes that would violate standards.

Static Random Access Memory-based Field Programmable Gate Arrays have been widely used in recent decades. Due to its instability, SRAM cannot be used in FPGA systems that require strong security and fast power-on. Non-Volatile Memories address these issues. Traditional NVM devices like anti-fuse, E2PROM, and flash require high voltage and have limited logic compatibility. These devices limit logic density and raise FPGA integration costs. Emerging NVMs like MRAM, PRAM, and RRAM are scalable and logic compatible.

The author proposes a single-ended 6T SRAM cell [1]. This design seeks to reduce dynamic power usage during read and write operations by approximately 50%. This reduction is believed to be possible without increasing read and write latency or standby power usage. The shortened read access time range shows the design's ability to endure process changes. A prior work [2] presented soft error protected 10T SRAM cells with two variations that improved static noise margin (SNM) and low-voltage functioning. The study found that the NMOS stacked-10T cell had better read stability margin and soft