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ASIC Design and Implementation of 32 Bit Arithmetic and Logic Unit

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Abstract

Low power techniques are becoming more important as portable digital applications expand quickly and demand high speed and low power consumption. The ALU is the most crucial and essential component of a central processing unit, as well as numerous embedded systems and microprocessors. Designing a 32-bit ALU that combines an arithmetic unit and a logical unit is the task at hand. The logic unit performs logic operations AND, OR, XOR, and XNOR with the aid of the recommended CMOS technology, while the arithmetic unit does the arithmetic operations addition, subtraction, increment, and buffering operations. The arithmetic unit is constructed using the 4x1 MUX, 2x1 MUX, and full adder, and the 4x1 MUX, required logic gates, and 4x1 MUX are employed to create the logical unit. Using Cadence Virtuoso Gpdk 180nm Technology, the results of the simulation of the 32-bit ALU, the ideal delay, and the Power were calculated.

Keywords: ALU, CMOS, Energy Efficient, VLSI, Logic, Arithmetic, Mux.

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1. Introduction

Building circuits with cheap costs, low space requirements, and low power consumption has become more and more crucial in recent times in the VLSI sector. CMOS technology, utilizing fewer transistors, allows for the creation of the Arithmetic Logic Unit with reduced propagation delay, power consumption, and minimized physical space. The Arithmetic and Logic Unit is a processing unit used in high-speed, low-power application design. CMOS technology reduces the size of the power supplies and Ground connections and uses them as inputs to the transistors.

There have been many logical implementations of the whole adder unit. Each style of reasoning has advantages and disadvantages of its own. The typical static CMOS full adder is built on a usual CMOS constitution. When the right transistors and voltage are utilized, this adder provides a complete yield voltage sway.

Reduced power indulgence and increased rate entail optimization at all design levels. The appropriate path type and technique are key factors in low-power design. Rapid processing is the expected standard for the average customer. Power indulgence is an essential design factor for an increasing number of Very Large Scale Integration (VLSI) circuits. The power reduction method starts with the main circuit design element. An adder serves as the brain of an Arithmetic Logic Unit (ALU). The ALU executes a chain of functions via select inputs. A digital computer's arithmetic logic unit (ALU) is an essential part. One of the primary tasks that a central processing unit (CPU) must

perform for practically all data it processes is bit shifting routines. The ALU is built to carry out these tasks. For the bulk of digital circuit applications, increasing speed and decreasing power consumption are two essential properties. The performance of the system will depend on how quickly the various modules included in the design operate.

The other sections of the technical work are structured as given. Section 2 provides an overview of the related ALU work. Section 3 discusses the process of the proposed 32bit ALU. In section 4, the results are studied. Section 5 provides the conclusion.

2. Related Studies

The ALU, as proposed [1], is a crucial part of the central processing unit. ALU feeds a 4x1 multiplexer inputs of logic '0' and '1'. The increment function is formed by logic '1' while the decrement function is formed by logic '0'. The one bit full adder, the 2x1 multiplexer, and the 4x1 multiplexer are the circuits required to create an arithmetic and logic unit. The complete adder, which is the only part of the 5-bit adder, generates six outputs: XOR, XNOR, AND, OR, SUM, and CARRY. ASIC design of multiplier is discussed [2, 3].

ALUs are designed for logical and numerical operation. It will incorporate addition, AND logic, XOR logic, and XNOR logic using a 4:1 multiplexer [4]. The BSIM4 model, which offers greater performance, will be used to effectively design all of the procedures for the tanning tool. The ALU's entire adder plays a critical role in the performance of the overall design. Reduced power usage from the ALU is largely due to the complete adder. The construction of a 32-bit ALU with less power consumption can be done more successfully with adiabatic logic. In order to reuse the energy contained, adiabatic logic achieves low power consumption by reducing the amount of current flowing through the components with the least amount of voltage drop in their capacitor [5]. The suggested ALU is designed with addition, subtraction, multiplication, shifting, comparison, AND, OR, NOT, and XOR [6]. This design strategy aims to produce digital circuits that use the least amount of power possible. The planned a new reversible logic section for a 4-bit binary 2's complement path and develop other low loss arithmetic circuits [7]. The output swing cannot be fully achieved even if the M-GDI approach uses a technology that is both energy and space efficient. On older circuits, a dangle restored M-GDI method was functional to solve this problem [8]. Sub circuit designs are made using novel techniques to create straightforward designs with improved ALU performance [9]. The creation of a 32-b arithmetic and log unit (ALU) that supports a delay-fault testability design-for-test (DFT) scheme that enables low-power operation [10]. It handles 32-bit bit-sliced data, which is separated into eight 4-bit slices. The bit-slice method lowers hardware costs and streamlines the circuit architecture [11][12]. A 32-bit ALU was designed using Verilog HDL with the logical gates and simulated in Xilinx software [13].

3. Proposed Methodology

An arithmetic logic unit (ALU), which performs arithmetic and logic operations on binary data, is built on combinational logic circuits. ALUs are crucial components of central processing units (CPUs) in computer systems. Here is a brief explanation of an ALU's basic architecture, which is depicted in Figure 1. The ALU receives a variety of inputs, including, the operands A and B of two binary numbers must be operated upon. A control signal or opcode, such as AND, OR, addition, or subtraction, that specifies the operation to be performed. Control signals are used for optional features or flags (such carry-in or overflow). The brain of the ALU is the combinational logic block, which, depending on the inputs and opcode, performs the selected operation. Equation circuits for addition and subtraction are often included. Circuits to do operations like bitwise AND, OR, XOR, and others. The ALU is do operation that may produce a binary number with the same width as the inputs. Status flags will represent conditions such as overflow, carry-out, and zero results. The flags sign (S), carry (C), overflow (V), and zero (Z) are often used. Based on the opcode, it determines which operation the ALU should do. The basic architecture of the ALU is implemented using flip-flops and digital logic gates which also produce the necessary functions for each operation. It is crucial to remember that modern processors may include highly optimized, pipelined ALUs that can accommodate various data lengths and have additional features for performance and efficiency. The design and complication of an ALU are notably inclined by the picky CPU style.

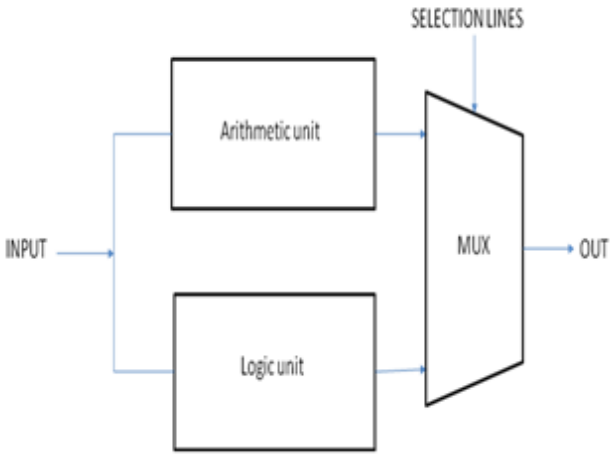


Figure 1. Basic Structure of ALU

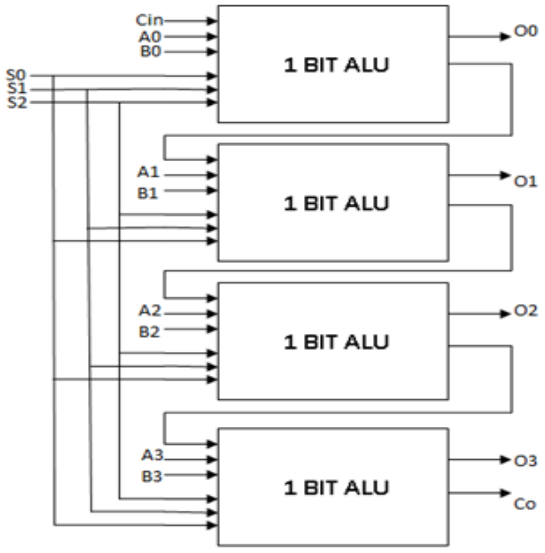
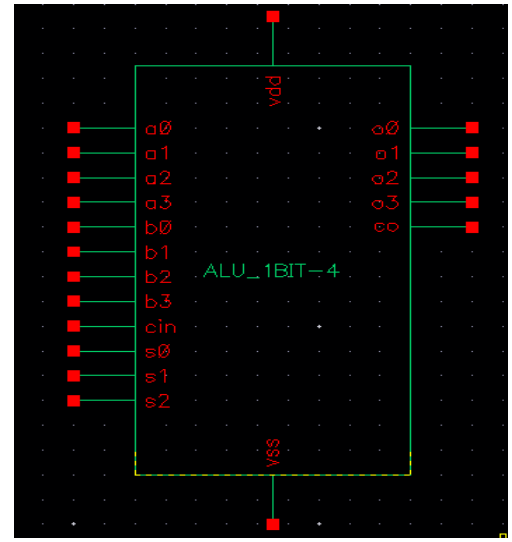


Figure 2. Block diagram of 4bit ALU

A logic unit is designed using AND, OR, XNOR, XOR CMOS logic gates, whilst an arithmetic unit is constructed using adder/Subtractor with buffer and multiplexer designed in. Various blocks of ALU are designed using CMOS gates and are combined to build 1bit ALU as per figure1.The designed 1bit ALU is used to design 4bit by combining four 1bit ALU as shown in Figure 2. Similarly 8 bit is designed by connecting two 4bit ALU together and Operations of 8bit ALU is listed in Table 1. Figure 3 shows block diagram of 8 bit ALU. The 16 bit ALU is generated using 8 bit ALU and similarly 16 bit ALU is formed.



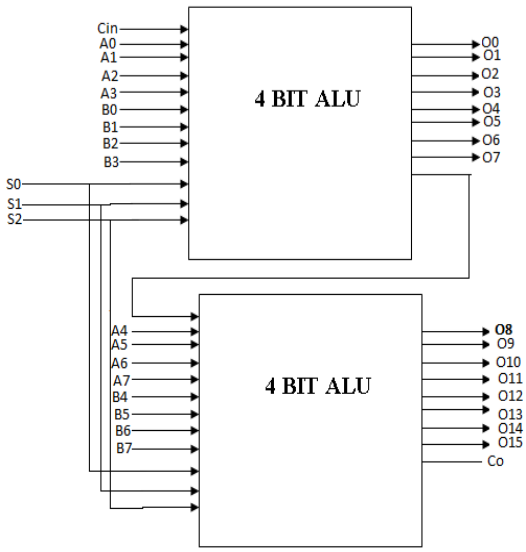


Figure 3. 4 bit ALU symbol and 8bit ALU

Table 1. Operations of 8bit ALU Design

INPUTS			OUTPUT
S0	S1	S2	
0	0	0	AND
0	0	1	OR
0	1	0	XNOR
0	1	1	XOR
1	0	0	ADDER/SUBTRACT
1	0	1	OR
1	1	0	A BUFFER
1	1	1	B BUFFER
			A’

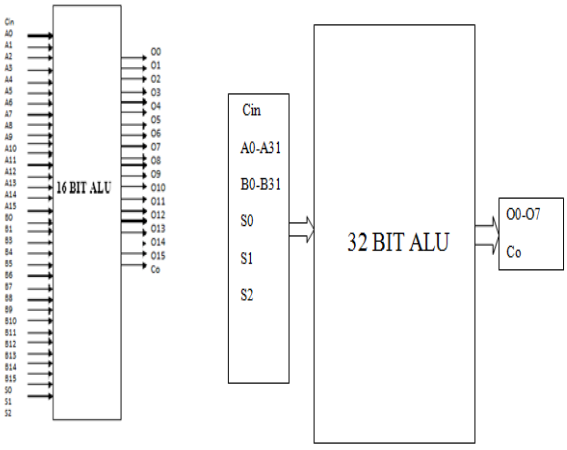


Figure 4. Block Diagram of 32 bit ALU

Every processor uses an arithmetic logic unit (ALU) for logical and arithmetic operations, being a crucial component of the digital system, found in a variety of devices such as computers, cell phones, and calculators. Using cadence virtuoso suite, a 32-bit ALU circuit was constructed, incorporating logical gates like AND and OR for each one-bit ALU circuit. 32 bit ALU is constructed using two 16bit ALU. Figure4 shows the block diagram of 32bit ALU and it has two 32bit input lines and selection lines to carry out logic, arithmetic operation. Selection lines are acted as control logic to perform ALU operation. It is possible to design any number of bits of ALU using the one bit ALU mentioned above. These 32-bit ALUs are designed to create 32-bit outputs for basic operations, 32-bit outputs for adder, and 32-bit remainders for subtraction operations. The 32-bit ALUs are designed to produce 32-bit outputs. By simply connecting two 16-bit ALUs in sequence and using the output carry of the previous ALU as the input carry for the current ALU, one can create a 32-bit basic ALU.

4. Results and Discussion

The ALU 1bit design is constructed using basic logic gates in CMOS logic and simulated using virtuoso suite. The schematic of Arithmetic unit and logic unit is shown in Figure 5. The simulated output is shown in Figure 6.

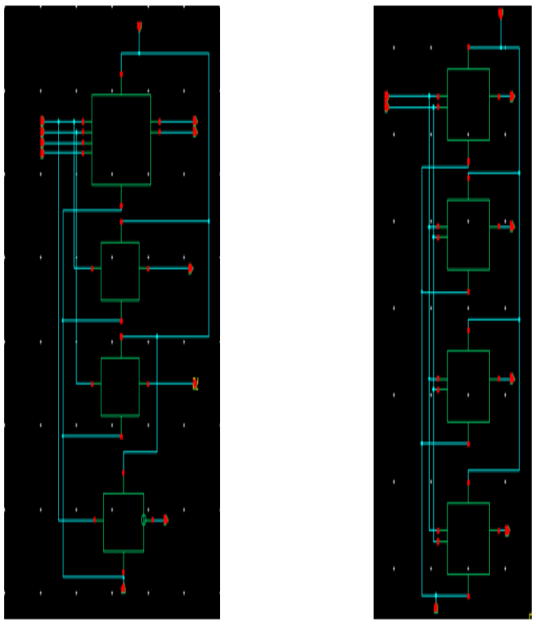


Figure 5. Schematic of Arithmetic unit and logic unit of 1bit ALU

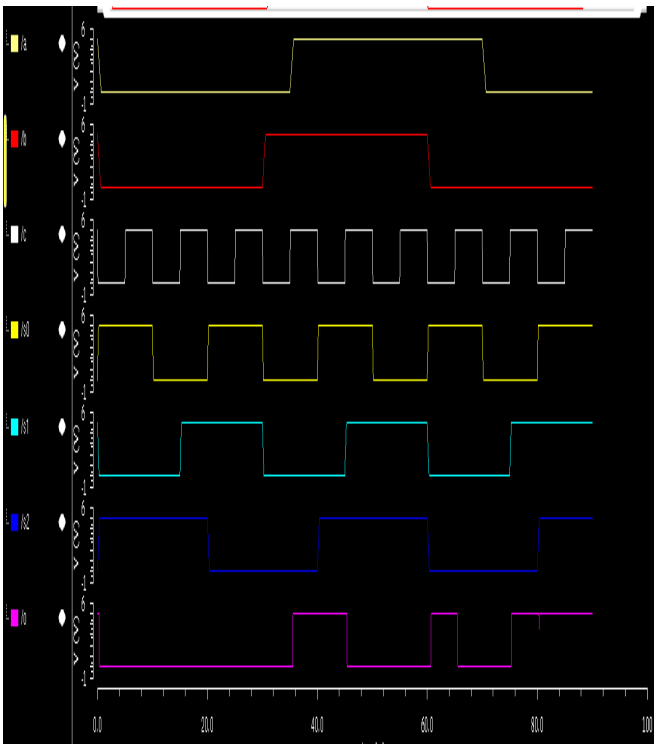


Figure 6. Simulated output of 1bit ALU

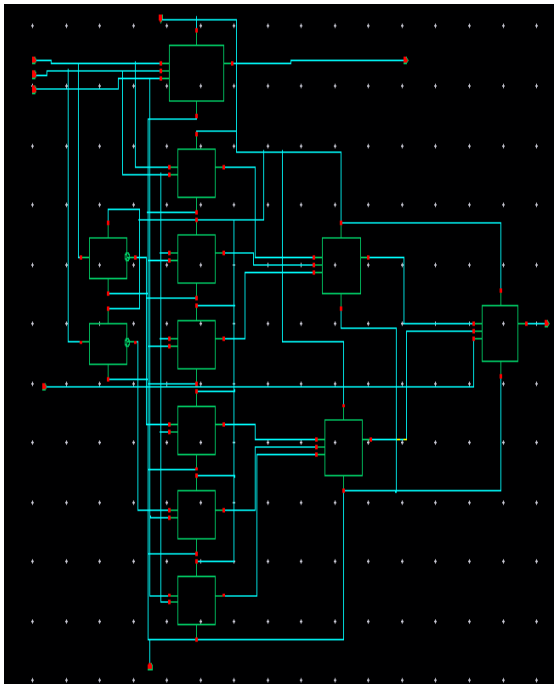


Figure 7. Schematic of Adder/Subractor

Figure 7 shows the schematic of Adder/Subtractor. The schematic of the 8bit ALU is shown in Figure 8, the schematic of the 16 bit ALU in Figure 9 and the schematic of the 32 bit ALU in Figure 10. The output waveform of the 32 bit ALU is obtained as shown in Figure 11.

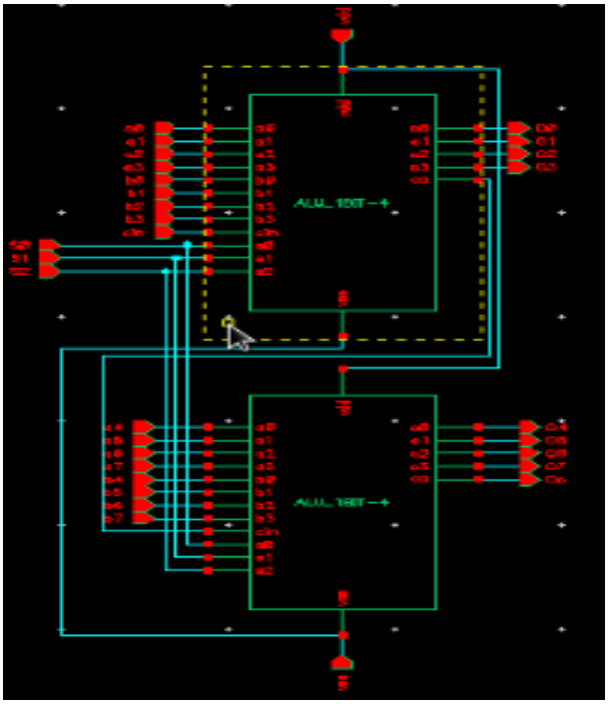


Figure 8. Schematic of 8 bit ALU

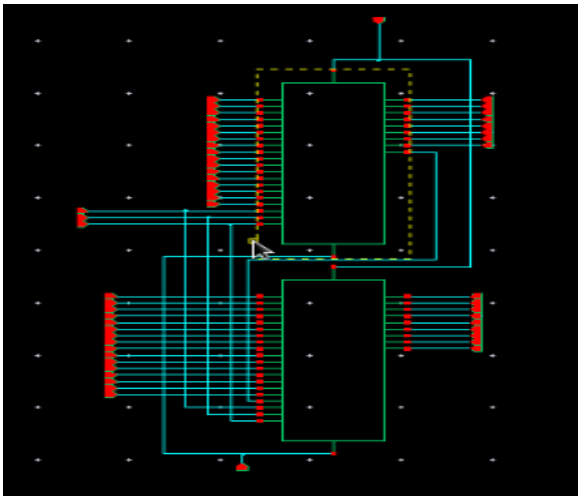


Figure 9. Schematic of 16 bit ALU

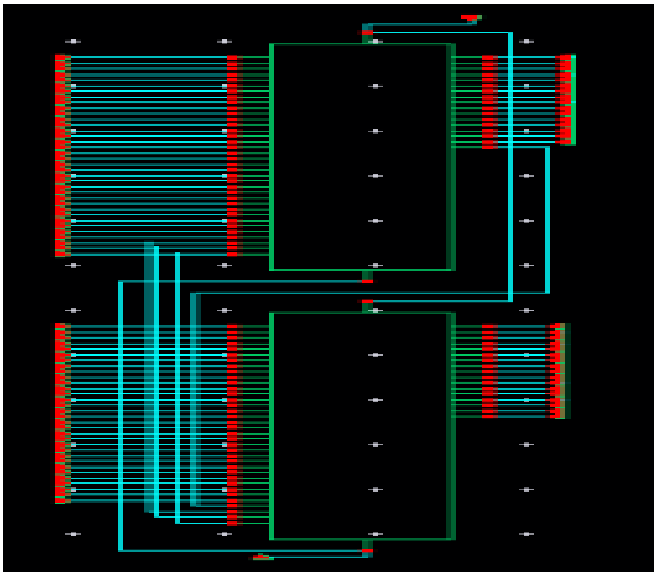


Figure 10. Schematic of 32 bit ALU

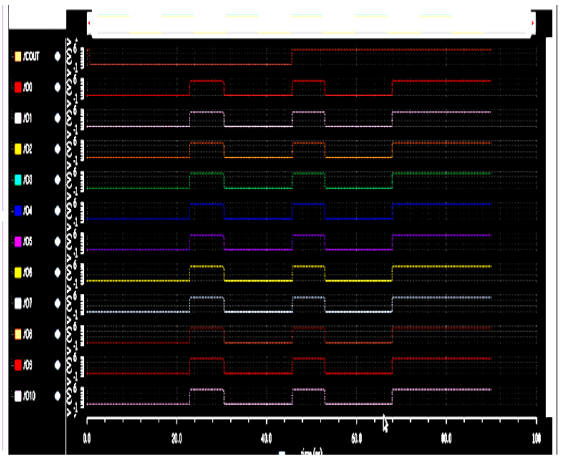


Figure 11. 32 bit ALU output waveform

Table 2. Power and delay of Proposed ALUs

ALU	Power(mw)	Delay(ps)
1 bit	0.0185	430.2
8 bit	1.066	342.4
16bit	2.199	297.6
32 bit	4.412	242.4

The power and delay of various adders are given in Table 2. The power is increases from 1 bit ALU is 18.47 mw and delay is 430.2ps and 32 bit ALU is 4.41mw and delay is 242.4. The high bit ALU is suitable for low power application.

Table 3. Performance of proposed ALU compared with existing methods

Design	Supply voltage (V)	Technology µm	Power Consumption(mw)	Operation Frequency GHz	Delay ps
Proposed	1.8	0.18	4.41	1.7	242.4
9[2019]	1.0	0.09	13.672	5	147.9
10[2005]	1.5	0.18	201	1.7	455
11[2001]	1.8	0.18	185	4	317
12[2005]	1.2	0.09	351	2.5	171
13[2016]	3.2	0.1	283	1.9	525
14[2018]	1.21.2	0.09	213	2	431

The performance of the proposed method was compared with existing as shown in Table 3. Power is less than existing methods [10] with slight rise in delay. Both power and delay are lower than other existing methods; the proposed performance is better suited for digital signal processing applications.

5. Conclusion

The 32-bit ALU features a logic unit for logical operations and an arithmetic unit for arithmetic operations. The 4x1 MUX, 2x1 MUX, and full adder are used to build the arithmetic unit and needed logic gates, and 4x1 MUX used to build the logical unit. The 32-bit ALU is designed using cascading processes from 1-bit ALU and simulated using Cadence Virtuoso Gpdk 180nm Technology. This design achieves low power consumption with a slight increase in delay, making it suitable for high-speed, low-power digital signal processing functions.

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