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A Power Efficient Based DC to DC Converter Using SCC

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Abstract

Scaling is one of the most important aspects and is considered for designing digital circuits. With the help of scaling techniques, it can integrate more features into the chip for optimization of actual circuit space. But the main drawback of this scaling is short channel effects. And also as the technology shrinks, the leakage power plays a crucial role compared to dynamic power consumption. To avoid leakage power, the proposed design technology is used for the optimization of power and for avoiding short channel effects. To further reduce power consumption, the CMOS technology is replaced with transmission gates in switched-capacitor converter circuits and GDI Technique while generating clock signals in the circuit for operations.

Keywords: FINFET technology, switched capacitor circuits, leakage power, transmission gates.

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1. Introduction

The average channel length has shrunk gradually due to the advantages of MOSFET and is fabricated for designing digital circuits. The main reason is MOSFET's are high speed and low area consumption. Innovation to overcome the barriers of quantum theory constraining the traditional MOSFET device structure is required to maintain the scale of the conventional bulk device. The most frequently mentioned limits are thickness and location control which is mentioned by high [Ion/ Ioff] ratio and Limitless pitch sub-thresholds and quantum mechanical tunnels of the carrier from drain to source and drain to tissue through with a narrow gate [1].

The channel depletion size must measure to include the off-state leakage by the layer thickness. This arises as a result of doping, which deteriorates the carrier's accessibility and ends up causing tunnel leakage at the end of the junction. In addition, the control of the dopant profile is more problematic in terms of depth and steepness [2]. To preserve gate control, correct voltage threshold, and quality, the gate oxide thickness is also required to be scaled with the channel length [15]. The diluting of the electrolytic gate causes gate tunneling leakage, which decreases the circuit efficiency, strength, and power output [3].

The thickness of the Si film must be less than 1/4 of the channel length to efficiently eliminate the off-state leakage. Select proper V_t by modifying the gate operations, for

example by using midgap or poly-SiGe [9]. At the same time, changes in material, such as the use of a) the high gate material and b) strained Si channel were aggressively sought for mobility and current driving development. There are several physical boundaries for scaling, even with the implementation of modern system architectures and materials, special and new circuit architecture problems remain [4].

The DC-DC switched mode Converters [1-3] are some of the simplistic electronic circuits that transform an electrical voltage level to another stage by switching operation [7]. In many digital circuits, the demand for all these converters has grown and is widely used for high-speed applications [8]. This is attributed to a broad spectrum of applications, such as mobile devices, computer peripherals, control of machinery, electronic equipment, DC engines, vehicles, aviation, etc. The key considerations are considered in the design for evaluation, regulation, and stabilization of switching converters [5].

A fixed voltage DC supply can be transformed into a DC variable voltage source in many industrial applications. A transformer of DC-DC is considered for DC converter and converted directly from DC-DC. A DC converter may be called DC equal to a constantly spinning AC transformer [9]. Like a capacitor, a DC voltage source may be down or upgraded. In electronic buses, trolley cars, sealift trucks, forklift trucks, and mine tractors, dc-dc converters are typically used for tractor control. They provide smooth, high productivity control and rapid dynamic response. DC-DC converters [4-6] can also be used to recycle the brakes of dc motors to restore energy into production. DC-DC converters are used for dc voltage control systems and have been used along with an inductor to produce the energy source again for DC source, mainly for the current source inverter [6].

2. Transmission Gate

In parallel, it can be build a simple, bilateral CMOS switch which is commonly known as a "Transmission Gate" to connect PMOS and NMOS devices [12].

The transmission gates vary slightly from conventional CMOS logic gates since the input and output gate is symmetrical or bilateral. The bilateral procedure is evident in the diagram below. The transmitting gate, with two superposed triangles representing the two signals in separate directions. So, here is a schematic of the simple circuit of the transmission gate and its symbol [13].

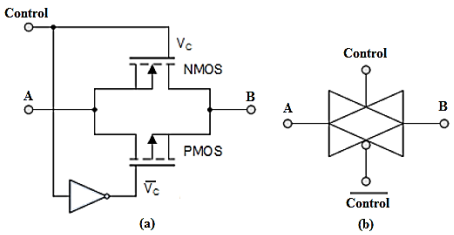

Figure 1. (a) Circuit Diagram of Transmission gate (b) Symbol of Transmission gate

In parallel to the inverter which provides two complementary signal voltages between the NMOS gate and the PMOS, two MOS transistors are connected back-to-back. When VC is LOW, the NMOS and PMOS are indeed cut off and the switch opened [14]. When the input control signal is LOW If the VC is high, the two transistors are biased and the switch is shut off. Therefore, if VC = 1, the gate functions as a 'locked' switch, and when VC = 0 is a voltage-controlled switch the gate is an 'opened' switch. The symbol bubble showing the PMOS FET gate [10].

The Transmission Gate (TG) is a bilateral interface with an input or output of each of its portals. The transmission gate has a third contact, called a control, in addition to the input and output terminals in which the control input specifies the switching status of its gate as both an open or closed switch [11].

In this, input is normally powered by a digital logic signal, which toggles between a fixed DC voltage and the ground (0V), generally Vdd, the switch is opened when control

entrance is low (Control = 0) and closed when the command input is HIGH (Control = 1) is shown in fig 1a&b.

3. GDI Technique

The need for growing speed, less area deployment, and low power dissipation induces various research efforts, due to the fast growth of portable digital applications. The ability to improve the outputs of the logical circuits, building on traditional CMOS technologies in the past two decades, contributes to the development of several logical modeling techniques. PTL - pass-transistor logic becomes the common type of logic in low-power digital circuits. Any of the key benefits of PTL in contrast to normal CMOS are (1) high-speed - attributable to the limited capacitance of nodes, (2) low power dissipation - because of smaller numbers of transistors, and (3). One of the fundamental problems of PTL is its up-to-date logic architecture uncertainty, which prohibits transistors from playing a significant role in real LSI logic. One of the principal factors is that PTL-based architecture does not have an easy and standardized cell Library. This study introduces a new low-power architecture methodology to solve much of the foregoing questions - the Gate Diffusion Input (GDI) technology. GDI requires a multitude of complex logic functions to be implemented for only two transistors. These approaches are designed with a small transistor quantity (in comparison with CMOS and PTL techniques) for fast, low-powered circuits while enabling easy top-down design with small cell libraries. Underneath is the simple GDI structure in fig 2.

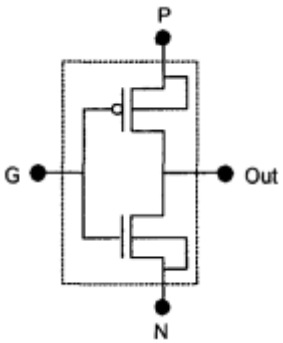

Figure 2. GDI basic cell

In Section II several similar works are briefly checked. The remainder of the paper is sorted as follows. Section III explains the proposed dc to dc converter; in section IV, findings are provided for comparison with the adder designs proposed and the current will eventually end the paper in Section V.

4. Related Work

At first, bulky and costly off-chip inductors were used by inducers-based switching control systems. Conventional DC-DC converters consisting of inductors are used in most commercially available systems. The inductor integration makes the design voluminous, loud, expensive and one of the heat-emitting components always [14]. The inductor is a major obstacle to compactness and cost as a result of a progressive tendency for high-temperature operations of converter systems [17]. There has been some effort to remove these bulky external inducers with spiral on-chip inductors or bonding wires. But chip inductor-based controls are impaired by errors due to improved inductor resistance and need more expensive production processes such as heavy metals or incorporation of ferrite core inducers on the chip [16]. An energy saving using CMOS and FinFET transistors are discussed in [22-24]. The power management for high speed devices are discussed in [20] and it uses FinFET technology for more power savings and its applications. The latest optimization system for power savings is PV and MPPT [18-19].

Receiving interest in both industry and the university, Switched Capacitor (SC) DC-DC Converters are now fully integrated on-chip by cutting off-chip inductors [12]. In SC DC-DC converters [7] MOS capacitors have been used to achieve low resistance and high-density capability and no accelerated development steps are needed. Figure showing the CMOS switched condenser system in fig 3.

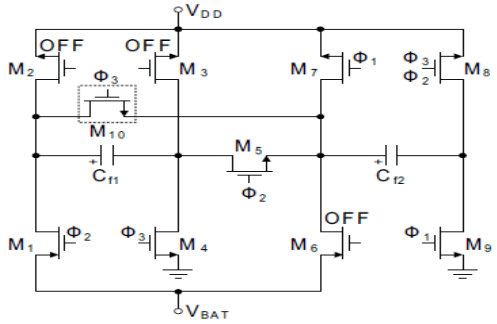

Figure 3. Existing CMOS switched capacitor circuit.

But the CMOS-Switched Converter is vulnerable to short channel consequences as the hardware declines. More energy loss is observed by the DC-to-DC converter with a CMOS-based switch capacitor converter [17].

5. Proposed DC to DC Converter

The Proposed Dc to Dc converter is planned to mitigate the short channel distortions in CMOS technology by using technologies.

Technology:

The layout of consisting of a silicone fin, which is usually a silicone insulator substrate, accompanied by a short or isolated gate on either side of the body. has two gates that could be controlled autonomously or at the same time. In one gate with the aid of voltage in the other gate, the voltage can be regulated. Systems will be used to improve efficiency by reducing the leaking current and power absorption, since both front and back gates can be worked individually but also at the same time.

In contrast with planar bulk systems, FinFETs have main advantages. The fact that the end height can be used to create a channel with a greater productive volume while still using a gate wrapping means that it exhibits the most current per unit of area than planar systems. FinFETs can achieve greater efficiency than bulk for given energy requirements or less power by their enhanced respective characteristics. There are two ways that the power savings can be achieved: decreased demand for large standard high-drive batteries, and the ability to work at a lower voltage with a certain volume of leakage.

Short channel effects become intolerable if the channel duration is limited relative to depletion areas. This limits the reduction in the gate length that is feasible. To minimize this effect, a channel length reduction of the depletion area width should be reduced. This can be accomplished either by increasing the concentration of channel doping or by increasing the potential or by both. The capacitance of the gate determines the power of the channel.

Eqn (1) shows that the capacitance of the gate can be enhanced by decreasing the production of the gate oxide. A system with thinner gate oxide has indeed been found to have decreased depletion width and therefore also strengthened SCE features[8].

Where,

$$C_{ox} = \frac{E_{ox}}{T_{ox}} \qquad (1)$$

C_{OX}: Gate Oxide Capacitance,

E_{OX}: Electric Field of oxide,

T_{OX}: Oxide Thickness

The following figure 4 a & b shows the settings for the Independent gate and shorted gate.

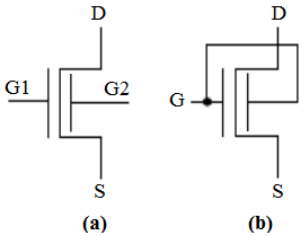

Figure 4. Different Classifications of (a) Independent Gate (IG), (b) Shorted Gate (SG)

The current twin-gate equation is given as [15]

$$Ids = u_{eff} W_{fin} q_i \frac{d_{vch}}{dy} \qquad (2)$$

$$u_{eff} = \frac{u_s}{1+us\left[\frac{vds}{v_{max}L_{eff}}\right]} \quad (3)$$

Where q_i is the inversion layer charge, V_{ch} is the quasi-fermi potential in the channel, u_{eff} is the effective surface mobility, W_{fin} is the width of the finfet. The inversion charge in the channel can be conveyed as

$$q_i = n_1 log\,[1 + ex\,p\,\frac{[(VG_1+(n_1-1)VG_2-V_T]}{n_1}] \quad (4)$$

Thus, V_{G1} and V_{G2} are therefore the front and rear gates. A new charging response is characterized as follows.

$$Ids = \frac{ueffw\left(1+\frac{qi}{n1}\right)dqi}{dy} \quad (5)$$

$$\text{Where } n_1 = 1+\left[\frac{C_{si}C_{ox2}}{C_{OX1}(C_{si}+C_{ox2})}\right] \quad (6)$$

The drain current is given after integration (5) from source to drain

$$Ids = \frac{ueffw}{Leff}\left[\frac{q_S{}^2-q_D{}^2}{2n_1} + (q_S - q_D)\right] \quad (7)$$

Where q_S and q_D are the regular load at source or drain. Replace V_{Ch} with the source and the drain voltage in an inversion charge equation for analytical charge at the source and drain.

The dc-to-dc converter is a collection of the gain selection, comparator, non-overlapping clock generator, and switched capacitor blocks. All these are applied with CMOS technologies in previous work, which has contributed to higher energy usage.

As dc-to-dc converters [9] are often used in portable electronics, the switched condenser converter is equipped with transmission gates for the reduction of electricity usage. GDI technology is used for non-overlap clock generation since the complex feature is largely only counted by 2 transistors. Therefore, compared with CMOS technology, transistor count and power consumption are decreased.

5.1. Comparator

Comparing the input signal with the referring signal, the comparator circuit produces the appropriate performance. The comparator device is designed by the technology to solve the issue of leakage power that dominates CMOS technology [10] nodes by developed model. Below fig 5 is the circuit diagram of the suggested model.

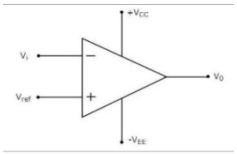

Figure 5. Comparator circuit

5.2 Gain selection block

As input to the selection block, the output of the comparator is given. The Gain selection block is built in proposed system to monitor the leakage capacity using the technology. The selection block circuit diagram is presented below fig 6.

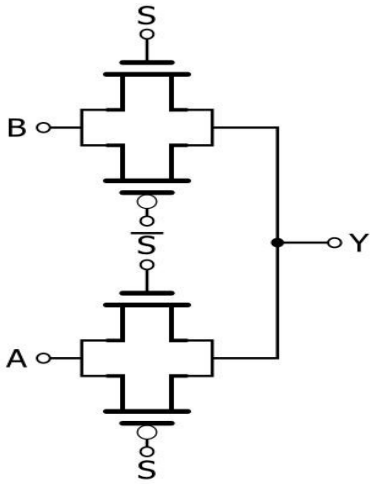

Figure 6. Circuit diagram of gain selection circuit.

5.3 Switched capacitor converter

The CMOS-based switched-capacitor converter [13] is replaced with transmission gates [12] based switched capacitor converter. Combining NMOS and PMOS in

transmission gates will solve the issue of greater resistance to switching and increased static power usage. Below is a description of the circuit diagram fig 7 &8 of the switch capacitor converter based on the transmission gate.

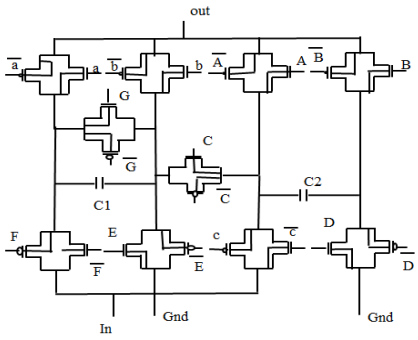

Figure 7. Circuit diagram of transmission gate-based switch capacitor converter using CMOS.

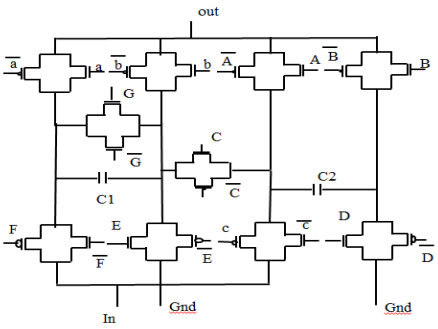

Figure 8. Circuit diagram of transmission gate-based switch capacitor converter using FINFET

5.4 Non overlap clock generator

The SCC switching relies primarily on the non-overlapping generator. Therefore, it is important to build a low-energy and effective clock generator. Thus, GDI [12] is replaced with the CMOS technology [14], to boost efficiency in terms of area and on power, and speed. Below fig 9 is the circuit diagram of the GDI technology non-overlapping clock generator.

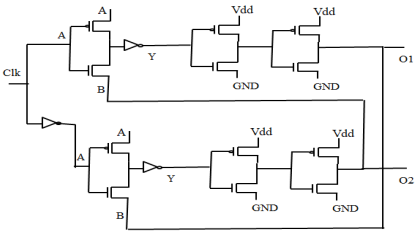

Figure 9. Non-overlapping clock generator circuit design using FINFET

5.5 FINFET based DC to DC Converter

Either the channel length should be improved or the technology should also be modified to address the short channel results. Growing/increasing the channel length implies no scaling. The design of CMOS has since been displaced by FINFET technology. Therefore, the total dc to dc converter circuit is generated using technology after developing the switched capacitor system with transmission gates and the non-overlap clock generator with the GDI technique [12]. The block diagram of FINFET based dc-to-dc converter will be seen below fig 10.

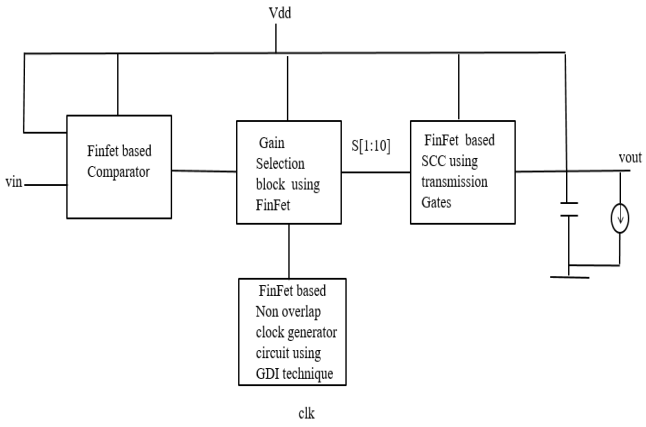

Figure 10. Block diagram of FINFET based DC to DC converter

6. Results and Discussion

The proposed dc to dc converter is designed using 32nm technology in cadence virtuoso and the simulation results are shown below fig 11 to 20. Although the transistor count of SCC is increased, there is a vast reduction in power. Since the dc-to-dc converter is mainly used in portable

devices where power is a major concern, the increase in area is acceptable.

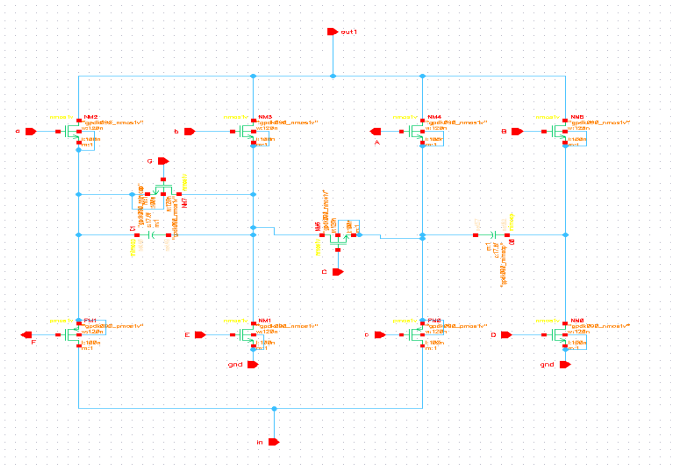

Figure 11. Schematic of existing switched capacitor converter

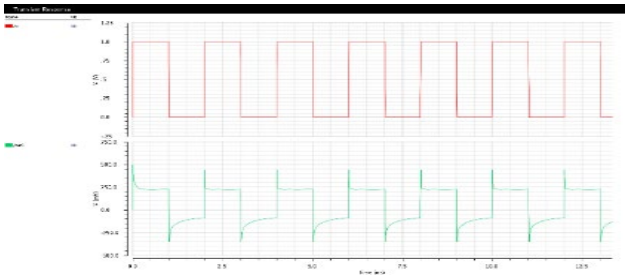

Figure 12. Output waveform of existing switched capacitor converter

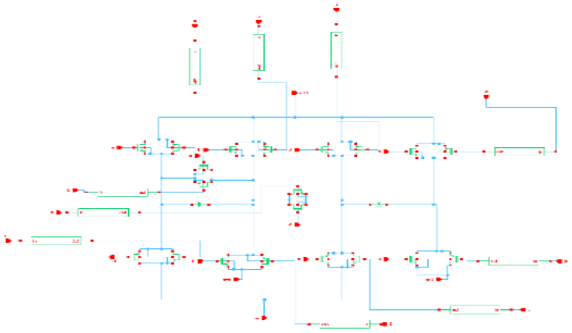

Figure 13. Schematic of proposed CMOS switched capacitor converter.

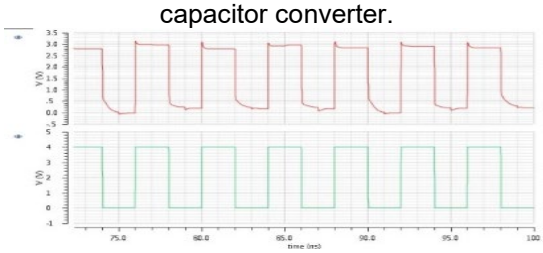

Figure 14. Output waveform of proposed CMOS switched capacitor converter.

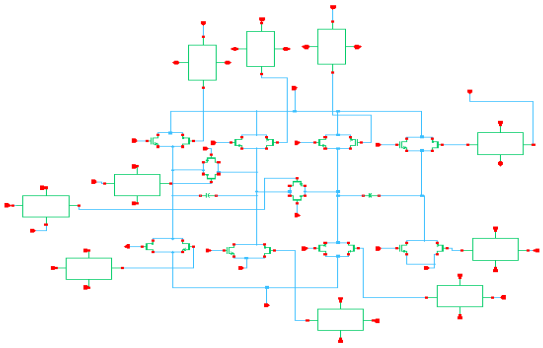

Figure 15. Schematic of switched capacitor converter using Transmission Gate.

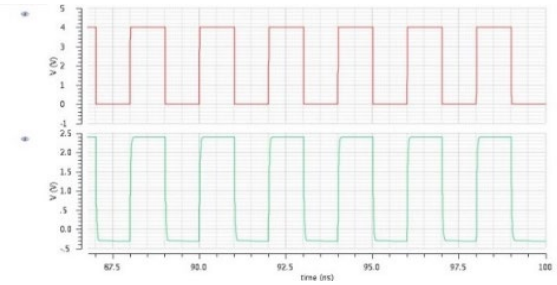

Figure 16. Output waveform of switched capacitor converter using Transmission Gate.

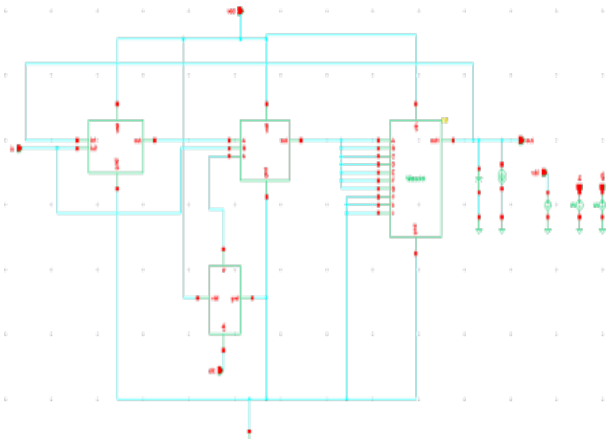

Figure 17. Schematic of proposed dc to dc converter

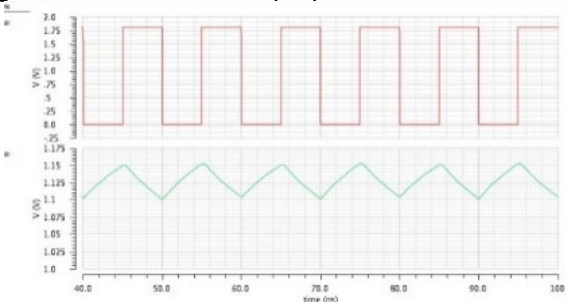

Figure 18. Output waveform of proposed dc to dc converter

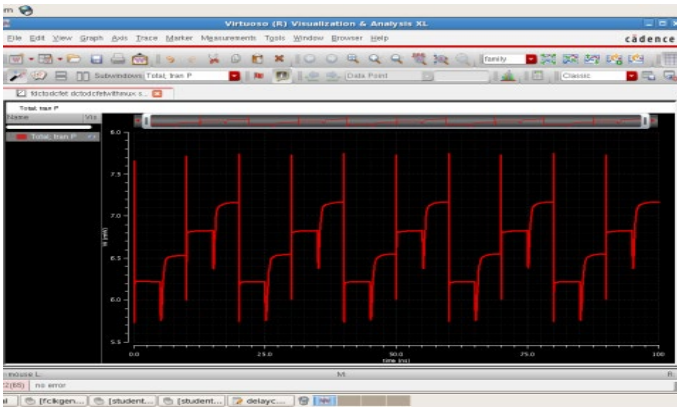

Figure 19. Power waveform for DC to DC converter

Improvement in terms of delay and power can be observed by implementing the proposed dc to dc converter when compared to existing converter. The based DC to DC converter design is presented in this paper. The results are shown in below table1, 2, 3 and 4

Table 1. Comparison between existing and proposed switched capacitor converter circuit

SWITCHED CAPACITOR CONVERTER	DELAY (ps)	POWER (w)
CMOS	2.8	78.01nw
Transmission Gates	1.42	28.29pw
transmission gates	0.6	8.13pw

The power consumption and delay required for conventional and proposed switched capacitor converter circuits given in the Table 1. It can be clearly observed from the Table 1, the power consumption and delay of the conventional CMOS based SCC is more compared to transmission gate SCC and power consumption and delay of FinFET Based SCC is less i.e. FinFET based SCC not only reduces the leakage power but also achieves high speed.

Table 2. Comparison between existing and proposed DC to DC converter circuit.

DC TO DC CONVERTER	DELAY (ns)	POWER
Existing CMOS	4.83	20nw
Proposed CMOS	4.12	15nw
transmission gates	0.701	26pw

From Table 2, delay and power parameters of the final dc to dc converter using CMOS, transmission gates and FinFET can be observed. It can be clearly observed that FinFET based dc to dc achieves high speed and less power dissipation.

Table 3. Comparison between existing and proposed switched capacitor converter circuit with input and output voltages.

INPUT VOLTAGE	CMOS (SCC)	TG (SCC)	FINFET (SCC)
5V	4.4	3.9	1.3
4V	3.5	2.9	2.4
2V	2.5	2.2	1.6
1V	0.8	0.6	0.3

Table 4. Comparison of various parameters between existing and proposed switched capacitor converter circuit

Method	Input Voltage	Technology	Output Voltage	Power	Output Regulation Method
Proposed FINFET	3	32	1.6	8.13 pw	hysteresis
Proposed CMOS	3	90	2.2	28.29 pw	hysteresis
Existing CMOS	3	90	2.5	78.1 nw	hysteresis
[7]	1.2	65	0.6	0.5 mw	PFM
[8]	1.2	130	0.4	0.125	Hysteresis+

				mw	body bias
[13]	1.8	45	1	7.2 mw	Hysteresis + capacitance modulation
[14]	1	65	0.47	4.7 mw	Hysteresis+ ripple control

It can be clearly observed that FINFET based dc to dc achieves high speed and less power dissipation. In table 4 proposed converter is compared with different previous methods. It can be clearly observed that when compared previous methods with regulation methods the proposed dc to dc converter consumes least power dissipation

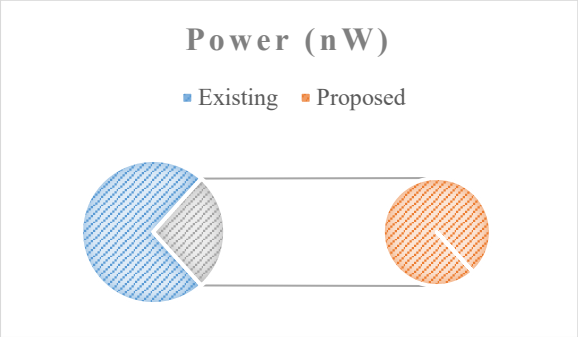

Figure 20. Comparison for existing SCC and proposed SCC

7. Conclusion

A low power dc to dc converter is designed using 32nm technology. By using the technology the short channel effects that occur due to technology shrinking are eliminated, which is the major concern in the existing dc to dc converter. Simulation results show that the proposed dc to dc converter shows better results in terms of power and delay.

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