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Experimental Validation of a Current-Source Converter with Reduced Dc-link Operating as Shunt Active Power Filter

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Abstract

Nowadays, the majority of electronic equipment behaves as nonlinear loads, introducing power quality problems into the power grid, namely, current harmonics and low power factor. These problems contribute to reduce the efficiency of the power grid and can cause malfunctioning of sensitive loads connected to the power grid. Therefore, it is important to develop power electronics solutions capable to mitigate these power quality problems. In this context, this paper presents a novel single-phase shunt active power filter (SAPF) based on a current-source converter, where the key differencing factor, when compared with the conventional approach, is the reduced dc-link. As the proposed topology requires a reduced dc-link, it represents a relevant advantage, requiring a less bulky inductance in the dc-link, reducing the losses, cost, and volume. The proposed SAPF with reduced dc-link is introduced in detail along the paper, and a comprehensive comparison with the conventional SAPF is established based on computer simulations. Besides, an experimental validation is carried out with a developed laboratory prototype, validating the main advantages of the proposed SAPF with reduced dc-link.

Keywords: Current-Source Converter, Shunt Active Power Filter, Power Quality.

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1. Introduction

The increasing use of the power converters contributes to the deterioration of the voltage and current waveforms of the power grid, which causes higher costs due to the incorrect functioning of the equipment connected to the power grid [1][2]. Due to the necessity of the use of the equipment more efficient and cheaper, the loads widely used are non-linear. When these types of loads are connected to the power grid, they consume non-sinusoidal currents, i.e., containing harmonics. As can be seen, it is important to develop power conditioners capable to mitigate these power quality problems. The shunt active power filter (SAPF) is one of the solutions to mitigate these power quality problems, being used for compensating the power factor, the current harmonics, and the current unbalances in a three-phase power grid [3]-[5]. In addition, as presented in [6] and [7], to mitigate the power quality problems, the SAPF can also be used for interfacing renewable energy sources with the power grid. Moreover, as presented in [8], in [9] and in [10], the functionalities of SAPF can be incorporated in electric vehicle battery chargers, representing a relevant contribution for the future smart grids, where the electric vehicle can act as a dynamic controllable load in the power grid.

Concerning the structure of the SAPF, depending on the dc-link constitution, it can be classified as a voltage-source or as a current-source [11]. A comparison between both structures for simple applications of SAPF is presented in [12] and for applications of electric mobility is presented in [13]. Since the focus of this paper is the current-source, a more detailed explanation is provided for this structure.

The current-source SAPF is composed of a coupling capacitor-coil (CL) filter with the power grid and by an

inductor in the dc-link. The dc-ac power converter is composed of semiconductors totally controlled such as Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Insulated Gate Bipolar Transistors (IGBTs), or Reverse Blocking-IGBTs (RB-IGBTs). These devices, in comparison with gate turn-off thyristors and bipolar junction transistors, can operate with higher switching frequencies, requiring smaller output passive filters, translating into more efficient, compact and cheaper solutions. In addition, the input impedance is higher, which results in low power consumption in the gate driver circuits [14]. However, when using IGBTs, it is needed to connect them in series with diodes, in order to ensure reverse-blocking capacity, thus it is avoided that the current flows by the antiparallel-diodes of IGBTs. In other words, when the IGBTs are conducting and the diodes are directly polarized, a unidirectional power flow is guaranteed. However, an alternative to this method consists in replace the IGBTs with the diodes in series by RB-IGBTs, where the use of diodes becomes unnecessary [15][16]. This type of SAPF has easy short-circuit protection, an excellent current control capability and high efficiency with low power loads over voltage-source SAPF [17]. However, the current-source SAPF needs an inductor in dc-link with a high inductance value, which is necessary to reduce the ripple in dc-link current for an acceptable value.

The main contribution of this paper is related with an innovative topology of a single-phase SAPF based on a current-source inverter with reduced dc-link. Moreover, the operation losses are reduced as well as the dimensions and the costs of the component. On the other hand, an inductor with reduced inductance value in dc-link allows a faster current control and thus, the average value of current can be minimized. This paper is an extension of the paper [18], where is explained in detail the control system of the final prototype. In this context, the main contributions of this paper are: (a) A novel topology for a SAPF based on a current-source power converter with reduced dc-link; (b) A SAPF constituted by RB-IGBTs in the main power electronics converter; (c) An experimental validation of the proposed SAPF.

2. SAPF with Reduced Dc-link: Proposed Topology

As described in the introduction, the main contribution of this paper is related with the proposal of an innovative topology to reduce the dc-link inductor of a SAPF based on current-source converter. For this purpose, it is adopted a topology of a current-source inverter with a modified dc-link. This topology consists of a hybrid energy storage, composed of one inductor, one capacitor, two diodes, and two IGBTs [19]. The conventional topology of a single-phase current-source SAPF based on RB-IGBTs is presented in Figure 1, while the proposed single-phase current-source SAPF with reduced dc-link is presented in Figure 2. Concerning the reduced dc-link, it is shown the dc-dc power converter in series with the dc-link of the single-phase current-source SAPF. Therefore, the power exchange is performed between the power grid and the dc-link, i.e., with the inductor and the capacitor (through the dc-dc converter). Thus, the inductance value of the inductor can be reduced.

As shown in Figure 2, the main differentiating factor of the proposed topology resides in the configuration of the dc-link. However, also the coupling filter with the power grid is different from the conventional solution of CL filter as presented, in [20]. In order to reduce the losses and electromagnetic interferences caused by the current-source converter, a passive damping filter is needed. In this type of filter, it is used a capacitor in series with the damping resistance to reduce its power dissipation [21]. The calculation of the capacitors value is determined in (1).

$$C_2 = n\, C_1 \tag{1}$$

Normally, it is considered a n value of 1, as it can be verified in [20], so the value of the capacitors in this filter have the same value, 10 µF. In (2), it is presented the calculation for the resistance R_d. The value of L is the sum of L_1 with L_2, whereas the value C is the sum of C_1 with C_2.

$$R_d = \sqrt{\frac{L}{C}}\sqrt{\frac{(2+n)(4+3n)}{2n^2\,(4+n)}} \tag{2}$$

Considering an inductive value L of 200 µH, the capacitors C_1 and C_2 with a value of 10 µF and n value of 1, the resistance value in this passive damping filter is 4.58 Ω.

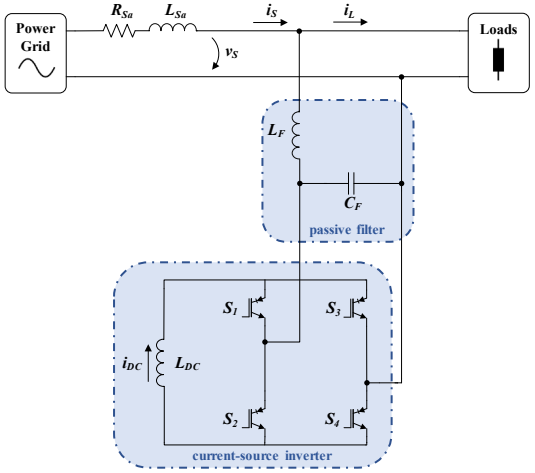


Figure 1. Electrical schematic of the conventional single-phase SAPF based on a current-source inverter.

3. Proposed Control Algorithm

Concerning the simulation of the dc-dc converter, the first step consists in calculate the loads active power. By multiplying the load current by the fundamental component of the load voltage obtained through the EPLL [22] algorithm it is obtained the instantaneous power, p. Subsequently, using a sliding average algorithm, it is possible to obtain the

average value, $\bar{p}$. Then, the calculation of the oscillating component of the instantaneous power is determined by (3).

$$\tilde{p} = p - \bar{p} \tag{3}$$

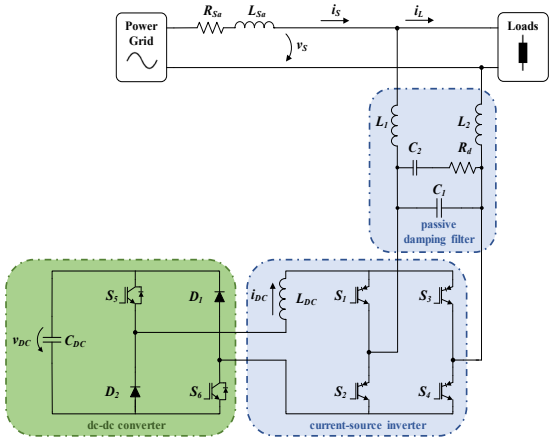


Figure 2. Electrical schematic of the proposed topology of the single-phase SAPF based on current-source inverter with reduced dc-link.

After the calculation of the oscillating power, $\tilde{p}$, it is possible to obtain the reference voltage for the dc-dc converter, $v_{out}{}^{*}$, dividing $\tilde{p}$ by the current value measured in inductor of dc-link, i_{DC}, such as represented in (4).

$$v_{out}{}^{*} = \frac{\tilde{p}}{i_{DC}} \tag{4}$$

The modulation of the converter is performed with a fixed switching frequency of 40 kHz, with three switching states: $+v_{DC}$, 0 and $-v_{DC}$. If the reference voltage, $v_{out}{}^{*}$, is positive, both IGBTs S_5 and S_6, represented in Figure 2, are enabled and the instantaneous output voltage, v_{out}, is equal to $+v_{DC}$, whereas if the reference voltage is negative, the IGBTs S_5 and S_6 are disabled and the instantaneous output voltage v_{out} is equal to $-v_{DC}$. The instantaneous output voltage value, v_{out}, is zero when only one IGBT, S_5 or S_6, is enabled. The operation states of the dc-dc converter are presented in Table 1.

Table 1. Operation states of the dc-dc converter.

State	S_5	S_6	v_{out}
1	1	1	$+v_{DC}$
2	0	0	$-v_{DC}$
3	1	0	0
4	0	1	0

In Figure 3, it is presented the block diagram of the entire control developed for the correct operation of the proposed topology. The synchronized voltage v_{PLL} with the power grid voltage is obtained through the EPLL, whose value is used in conjunction with the load current, i_L for the calculation of the compensation current i_c, applying the Fryze theory. On the other hand, it is obtained the regulation power p_{reg} necessary for the regulation of the dc-link of the current-source inverter using the PI controller. Based in the regulation power p_{reg} and the power grid voltage v_S, it is determined a regulation current i_{reg}. Adding i_{reg} and i_c results in the reference signal which is used to be compared with carrier waveform of 40 kHz, where the pulse-width modulation (PWM) signals for the power semiconductors of the current-source inverter are defined

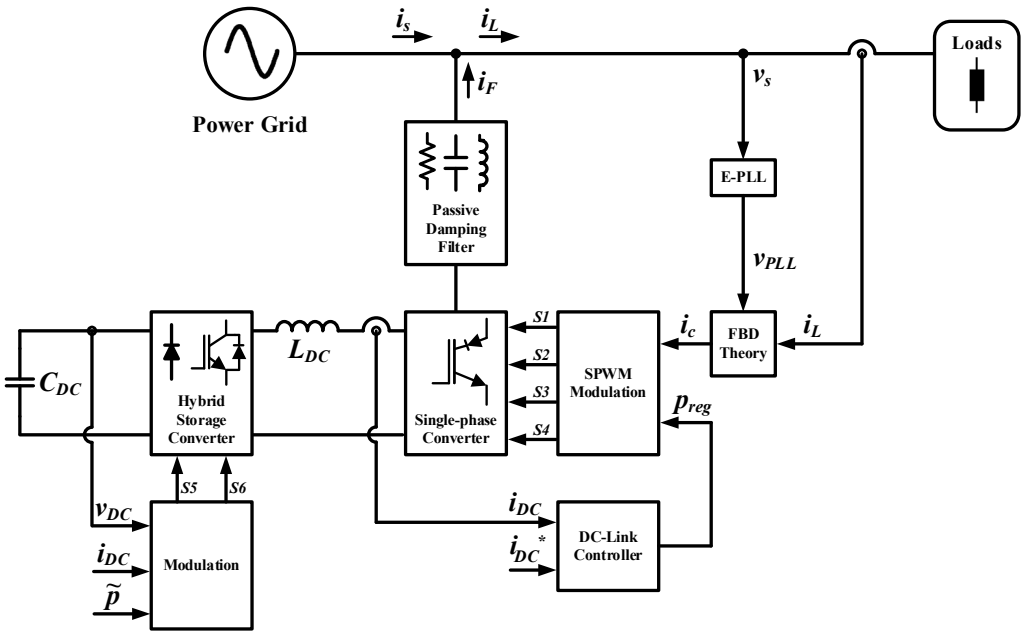


Figure 3. Block diagram of the single-phase SAPF based on a current-source inverter with reduced dc-link control algorithms.

through the unipolar sinusoidal PWM. As described above, the reference voltage v_{out}^{*} is determined applying the equation (4) using the value of i_{DC} and $\tilde{p}$, that is subsequently compared with the measured voltage in dc-link of the dc-dc converter, v_{DC}.

The proposed topology allows to reduce the inductance value of the inductor in dc-link of the inverter, since the dc-dc converter stores most of the energy which was stored exclusively by the inductor [19]. In order to demonstrate the operation principle of the proposed topology, key computer simulation results were obtained for the conventional SAPF, represented in Figure 1, and for the proposed SAPF with modified dc-link, represented in Figure 2, where were considered inductors, L_{DC}, of 200 mH and 50 mH, respectively. Figure 4 shows the current in dc-link in both topologies, whose current regulation was made through a PI controller presented in [23], for a reference of 20 A. It is important to note that the gains of the PI controller influence the overshoot observed in both simulation results. As it can be seen, the current stabilizes for the required reference of current at the instant 0.25 ms.

Figure 5 shows the voltage, v_{DC}, in the capacitor of the dc-dc converter, where it can be observed that, since the instant 0.2 s the dc-dc power converter is activated and the capacitor C_{DC} starts storing energy, with a maximum voltage of approximately 400 V. Since part of the energy is stored in the capacitor, the inductor of the inverter does not need a huge inductance value, representing the key advantage of the proposed topology.

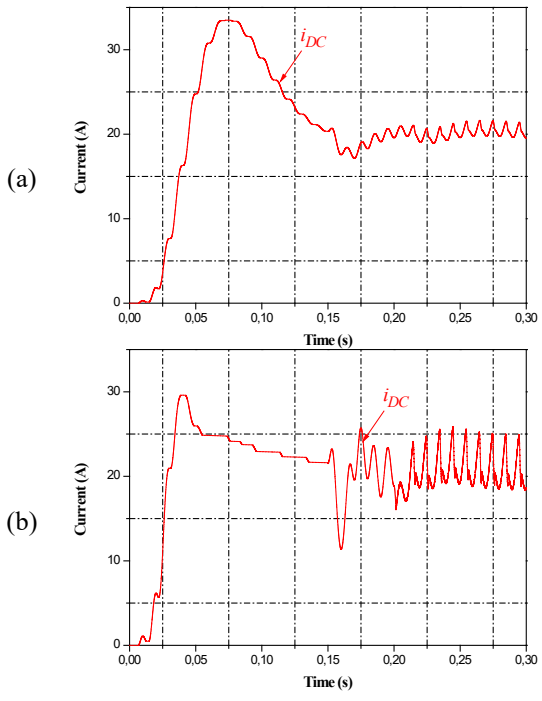


Figure 4. Simulation results of dc-link current, i_{DC}, regulation: (a) Conventional SAPF;(b) SAPF with reduced dc-link.

Considering both topologies, simulation results were also obtained to analyse the compensation of power quality problems. Therefore, at the time 0.22 s, similar loads are connected in both simulations. Figure 6 shows the power grid voltage, v_S, and the load current, i_L, where it can be observed that the current is delayed in relation to the voltage and presents a Total Harmonic Distortion in relation to the fundamental component (THD$_{\%f}$) of 36.45 %.

Figure 7 (a) shows the compensation current produced by both SAPFs. The behaviour of Fryze theory can be proven by subtracting the current consumed by loads, i_L, by the reference compensation current, i_c^{*}, resulting in the theoretical current in the source, as it is showed in Figure 7 (b) and Figure 7 (c).

As the current consumed by loads, i_L, introduces current harmonics in the power grid, it is necessary the injection of the compensation current produced by the SAPF, which in this case is obtained through the Fryze theory [24][25].

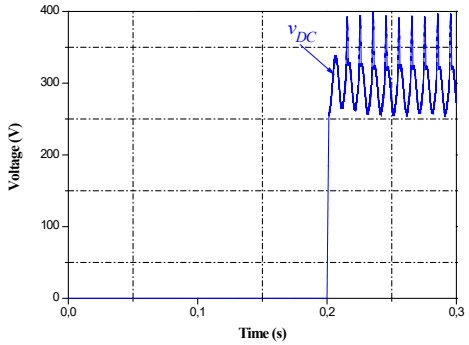


Figure 5. Simulation result of the dc-link regulation of the proposed dc-dc power converter SAPF with reduced dc-link.

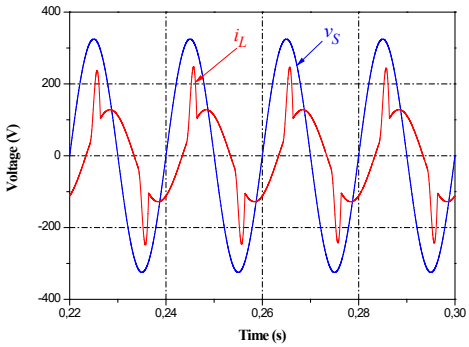


Figure 6. Simulation results of the power grid voltage, v_S, and the load current, i_L, in both topologies.

Finally, in Figure 8 (a) are illustrated the power grid voltage, v_S, and source current, i_S, after the compensation with the conventional SAPF, where the THD$_{\%f}$ of current is reduced to 4.25 %. On the other hand, as shown in Figure 8 (b), with the proposed SAPF with reduced dc-link, the source current, i_S, is also almost sinusoidal, presenting a slightly higher THD$_{\%f}$ of 7.78 %.

4. Evaluation and Comparison of the SAPF with Reduced Dc-link

With the aid of the computer simulations it is possible to compare the conventional with the proposed SAPF with reduced dc-link in more detail. In Table 2 are presented the inductance values used in both simulations, the $THD_{\%f}$ and the power factor (PF). As can be observed, the inductance of the inductor in dc-link used in the SAPF with reduced dc-link is four times lower in comparison with the inductor that composes the dc-link of the conventional SAPF. On the other hand, in both simulations, it is obtained a unitary PF. However, the $THD_{\%f}$ is somewhat higher than the obtained in the conventional SAPF, due to the low inductance value in the dc-link. Analysing the simulation results, it can be concluded that the proposed topology has more advantages, once it was proved that it is possible to reduce the inductance value of the inductor in dc-link of the current-source inverter.

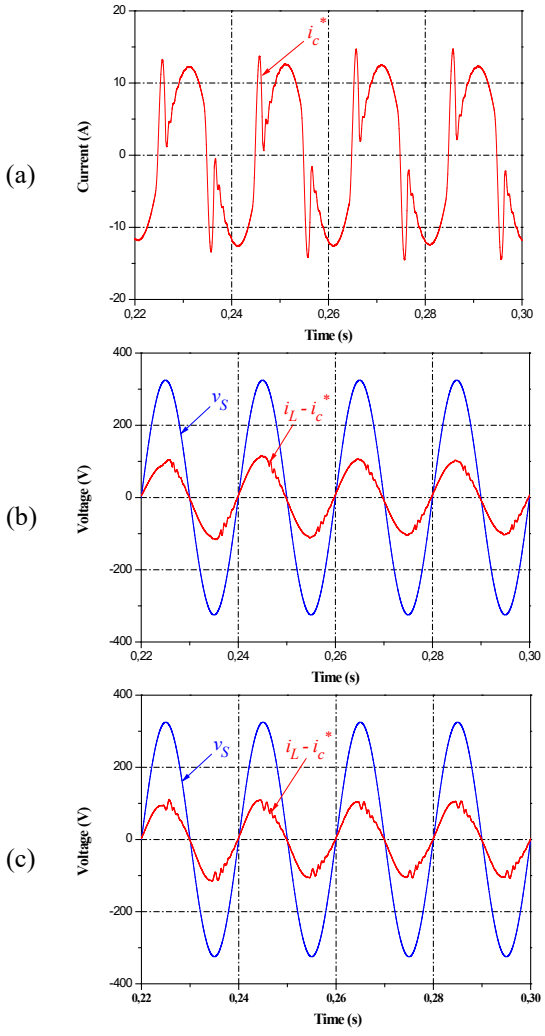


Figure 7. Simulation results: (a) Reference compensation current produced by the Fryze theory, (b) Theoretical source current after compensation for the conventional SAPF; (c) Theoretical source current after compensation for the proposed SAPF with reduced dc-link.

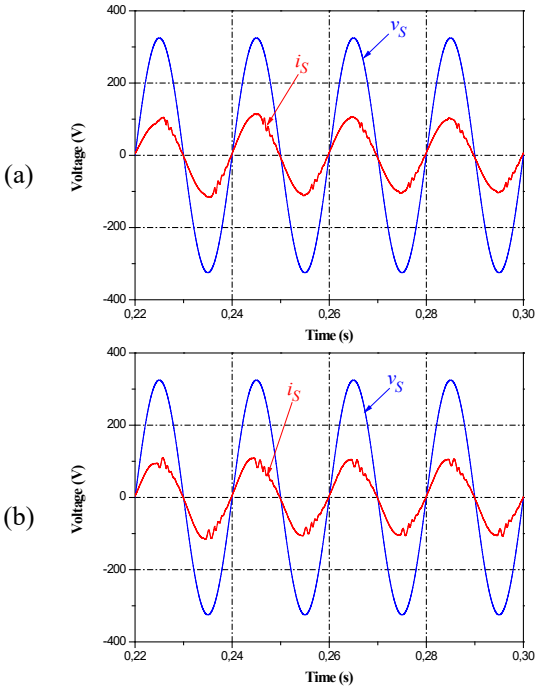


Figure 8. Simulation results of the power grid voltage, v_S, and source current, i_S, after compensation: (a) Conventional SAPF; (b) Proposed SAPF with reduced dc-link.

Table 2. Comparison between the conventional SAPF and the proposed SAPF with reduced dc-link.

Parameters	Conventional SAPF	SAPF with Reduced Dc-link
Inductance(mH)	200	50
$THD_{\%f}$ (%)	4.25	7.78
PF	0.99	0.99

After validating the operation principle of the proposed topology, a prototype of the dc-dc converter and the single-phase current-source inverter was developed (Figure 9). Thereafter, are presented the main experimental results obtained for the proposed SAPF with reduced dc-link. The current-source inverter is composed by two legs with two RB-IGBTs (Fuji Electric, model FGW85N60RB) in each leg. In each RB-IGBT is connected to a protection circuit against overvoltage. Besides that, in order to ensure the protection of the inverter, are connected varistors in parallel with the RB-IGBTs and in parallel with the dc-link, whose actuation voltage is 510 V. On the other hand, the dc-dc converter consists of two IGBTs (Fairchild Semiconductor, model FGA25N120ANTD). The protection circuit of these semiconductors are similar to the RB-IGBTs of the inverter. In each leg, the IGBTs are connected in series with one diode (IXYS, model DSEP 29-12). For the dc-link voltage, it was defined a nominal voltage of 400 V and nominal capacitance of 100 µF, resulting in a dc-link composed of five capacitors

of 20 µF (Vishay, model MKP1848C) connected in parallel. Moreover, it was developed three driver boards, two of them to actuate the RB-IGBTs and one to actuate the IGBTs of the dc-dc converter. The driver boards used to the current-source inverter generates the overlap-time needed for the correct operation of the inverter.

Moreover, it is crucial the development of a control system for the implementation of the control algorithms previously simulated in software PSIM. In Figure 10, it is shown the control system developed for the final prototype. The control system is composed by digital signal processor (DSP) board, command boards, voltage and current sensors boards and signal conditioning board. In this project, the DSP board used is the *TMS320F28335* from Texas Instruments [26]. The signal conditioning board aims at adjusting the output signals of the voltage and current sensors to the values allowed by the internal ADC of the DSP. The signal conditioning is carried out for 16 channels of ADC, where 6 channels of the ADC were used, since the system has 6 sensors, 3 voltage sensors and 3 current sensors. In addition, this board has a circuit for the detection of errors in order to guarantee that the system operates within acceptable values. If the signal of a sensor exceeds the predefined limits, it will be generated an error signal that disables the commutation of the power semiconductors to avoid the damage of the power converters. In Figure 10, it is shown the DSP board which is connected to the signal conditioning board (placed under). For this project, it was used two command boards, one for the current-source converter and another one for the dc-dc converter. The aim of these boards is to adapt the signals levels from 3.3 V from the DSP to 15 V of the IGBT gate driver circuits and enable or disable the commutations of the power semiconductors of both converters.

Figure 11 shows the power grid voltage, v_S, and the signal generated by the EPLL, v_{PLL}. It should be noted that the transient verified, shows that the output signal of the EPLL, v_{PLL}, rapidly reaches the synchronism with the power grid voltage. Despite the power grid voltage being distorted, the output signal of the EPLL, v_{PLL}, is sinusoidal and in phase with the power grid fundamental voltage, as intended. To ensure the correct operation of the single-phase current-source inverter, it is necessary to establish an overlap-time between the two command signals. It is important to mention that only one superior semiconductor, S_1 or S_3, and inferior semiconductor, S_2 or S_4, are connected, except during the overlap-time. Therefore, when one of the superior semiconductors is open, the other superior semiconductor starts conducting, the same happens with the inferior semiconductors. In Figure 12, it can be observed the overlap-time with a duration of 1 µs between the two command signals. The duration of the overlap-time was selected based on the turn-on and turn-off times of the selected RB-IGBTs, ensuring that the current in dc-link is not interrupted. In order to verify the effectiveness of the Fryze theory, it is calculated the theoretical current in the power grid side, subtracting the measured current in load, i_L, from the compensation current reference, i_c^*. Therefore, the theoretical current in the grid side can be demonstrated through the MATH functionality available in oscilloscope, *Tektronix* TPS 2024, which allows the calculation previously

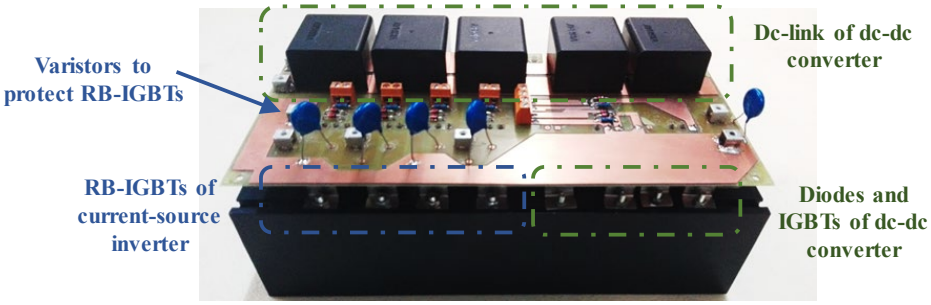


Figure 9. Final prototype of the dc-dc converter and single-phase current-source inverter fixed to heatsink.

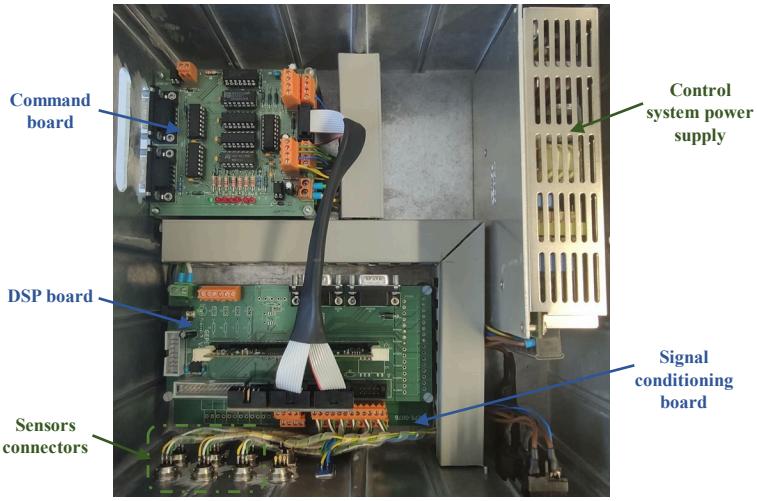


Figure 10. Final prototype of the control system.

described. Figure 13 shows the theoretical current in source, (i_L - i_c^*), the load current, i_L, the compensation current, i_c^*, and the signal generated by EPLL, v_{PLL}.

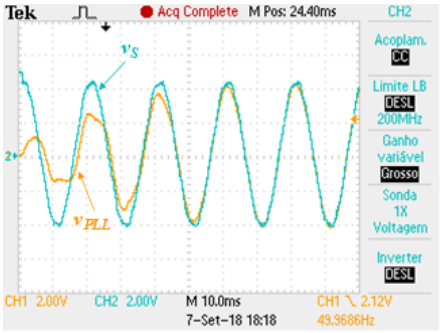
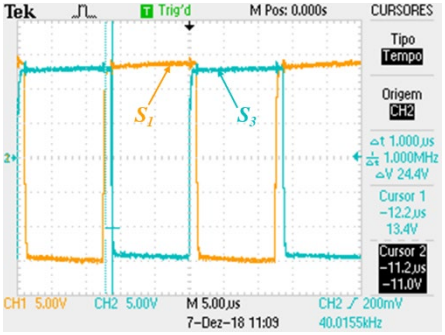


Figure 11. Experimental results of the proposed SAPF with reduced dc-link: Synchronism of the EPLL, v_{PLL}, with the power grid voltage, v_S.

(a)



(b)

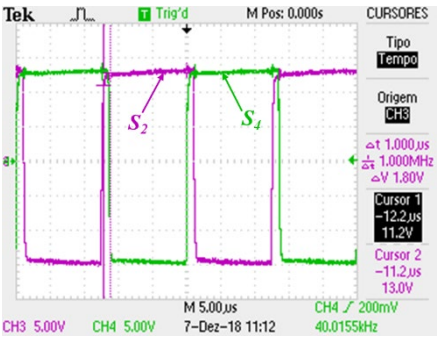


Figure 12. Experimental results of the proposed SAPF with reduced dc-link concerning the overlap-time of 1 µs between the gate signals of the semiconductors: (a) S_1 and S_3; (b) S_2 and S_4.

After that, it was performed the regulation of the current in dc-link of the current-source converter, applying the PI controller. The performance of the PI control technique is validated for a reference current of 2 A. Figure 14 illustrates the behaviour of the current in dc-link, i_{DC}, where it can be observed that the measured current in dc-link, i_{DC}, after the initial transient, follows perfectly the reference current, i^*. For this reason, it can be concluded that the control technique performs as intended.

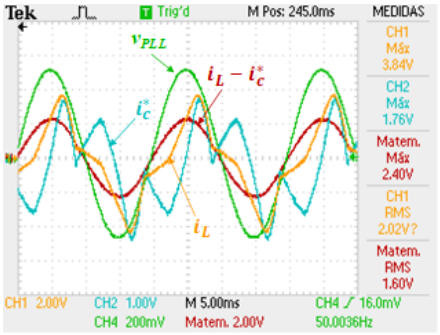


Figure 13. Experimental results of the proposed SAPF with reduced dc link concerning the Fryze theory: Load current, i_L; Compensation current reference, i^*_c; Theoretical source current, (i_L - i^*_c); Signal generated by the EPLL, v_{PLL}.

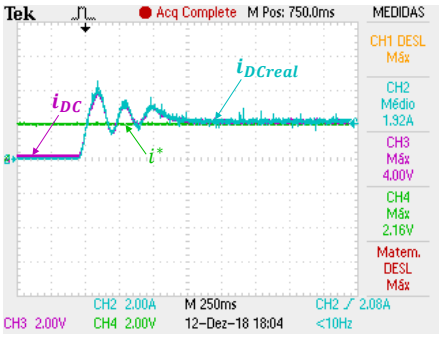


Figure 14. Experimental results of the proposed SAPF with reduced dc-link during the dc-link current regulation: Reference current, i^*; Dc-link current, i_{DC}.

5. Conclusions

This paper proposes a current-source shunt active power filter (SAPF) with reduced inductance in the dc-link, used for the compensation of current harmonics and power factor, with interface of a hybrid storage system which consists of a dc-dc converter connected to the current-source converter. The main purpose of the dc-dc converter is to store part of energy stored by the inductor of the current-source converter. Throughout the paper the performed simulations are described in detail and it is verified the possibility of reducing the value of the inductance to a considerably lower value. Moreover, this paper presents the operation principle of the dc-dc converter that has a crucial role in the proposed topology. Due to the hybrid energy storage strategy, part of the energy is stored by the capacitor of the dc-dc converter, and thus, it is not necessary to use a bulky inductor in the dc-link. In addition, this paper presents the power theory used for calculating the reference of the compensation current to be produced by the SAPF, and the reference voltage for the dc-dc converter. This paper also provides a concise explanation about the operation states of the proposed SAPF. A developed prototype is presented and described in detail, namely the power board that includes both power converters, and the boards that compose the control system. Finally, the

main experimental results are presented, in order to validate the correct operation of the proposed SAPF with reduced dc-link.

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