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Design and Analysis of Energy Efficient Domino Logic Architectures with Single Electron Transistors in Pull Down Network and Keeper Topology

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Abstract

Nanotechnology and VLSI goes hand in hand. Modernization of electronics and communication systems has demanded for compactness of the devices with low power and high speed. Conventionally CMOS logic is preferred due to its low power and its high speed benefits. Researches demand a new logic style that can effectively replace conventional CMOS. Many styles including Domino logic are already gaining attention in this regard. The proposed work introduces Single Electron Transistors (SET) instead of NMOS in Pull Down Network and Keeper transistor of Domino Logic. As SETs are predominant in Nanotechnology, when employed in domino logic circuits as a fusion with normal MOS transistors will contribute effectively in terms of area, power and delay. The parameters are estimated with Cadence 45nm (SET- Spice Model) technology. The proposed domino logic architectures come up with an average of 68% energy efficiency when compared with conventional CMOS circuit and its Domino logic predecessors.

Keywords: Energy Efficient Domino Logic Design, Single Electron Transistor, Nanotechnology

Received on 11 September 2020, accepted on 19 November 2020, published on 27 November 2020

doi: 10.4108/eai.27-11-2020.167287

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1. Introduction

Emerging fields such as Artificial Intelligence, Machine Learning, Deep Learning, and Data Science requires compact devices with energy efficient characteristics at all levels. This compactness in area and energy efficiency has been explored over the years by researches throughout the world. Conventional CMOS logic devices have been used extensively in all VLSI circuits for its low power dissipation capabilities. Many logic styles such as Pseudo NMOS Logic, Pass Transistor Logic, Dynamic Logic and Domino Logic are already in the process of CMOS Logic for few circuits. In the proposed work, Domino logic is explored with various enhancements and optimizations. Initially Domino logic with normal NMOS & PMOS transistors were analysed [5]. Later the key element in most Nanotechnology applications called Single Electron Transistor (SET) are used instead of NMOS transistors as a hybrid combination [1, 4] especially in the predominant parts of Domino Logic Style of design. This replacement has proved to be better in case of power, delay and area efficiency. This enhanced version of Domino logic style can be very helpful in applications which demand for compact circuits with good energy efficiency as well.

The research paper is organised as follows: Section 2 about an overview of SETs and their literature; Section 3 gives an insight on exploring Domino logic style of designing circuits; Section 4 deals with the idea behind proposed method. Section 5 deals with the advantage of using SET also in keeper transistor. Section 6 deals result and further inferences from the result. Section 7 concludes the paper and discusses about the future scope and research possibilities.

2. SETs- An Overview

Single Electron Transistors are more likely nano-crystals with nano-size diameter where the source and drain are

similar to normal MOSFETs except the channel which is replaced by a small dot like Tunnel Junction Diode. A vacuum or insulation layer is created by this Tunnel Junction Diode which gives the same gate capacitance (C_g) effect as that of normal MOSFET's. The gate voltage V_g is used to control the change on the Gate-Dot capacitance (C_g). The equivalent circuit of a SET and its symbolic representations are given in Figure 1. In Set, a very thin nearly 1nm thickness vacuum is the insulator which separates two piece of metals namely source and drain. The discrete electronic configuration of SET permits only one electron inside the tunnel with specific criteria. SET's are mainly explored for their faster performance than normal transmitters and can be widely explored in Single – electron memory and logic systems. But these sets can be implemented only for simple architectures. They suffer "offset charges" (i.e.,) the V_g (gate voltage) have to meet peak current which varies randomly from 1 device to other. This makes it highly impossible for complex circuits. Due to their unmatchable faster switching times, they can be implemented for denser & critical signal and image processing systems.

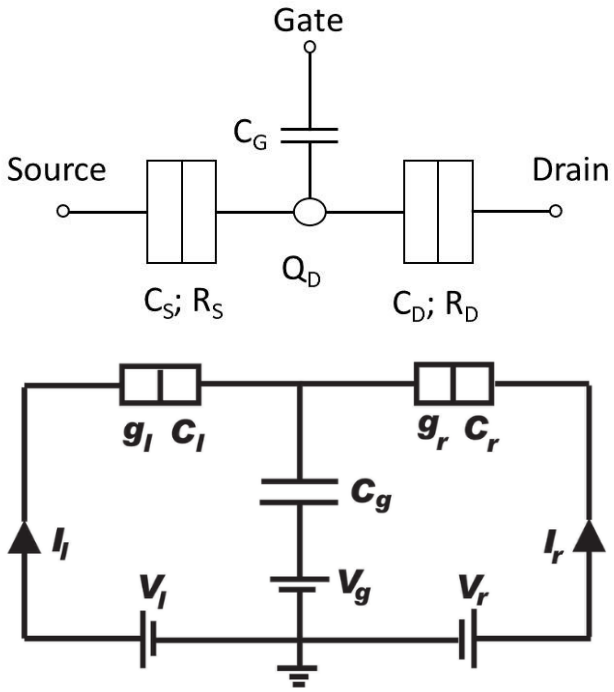

Figure 1. Symbolic representation and equivalent circuit of SET

SET research all started off with a hybrid SET-MOS architecture which was later converted to negative differential resistance architecture by shorting Gate and Drain terminals [1]. Another hybrid CMOS-SET circuit Monte Carlo Simulations were carried out to analyse its sustainability for CAD frameworks in designing IC's [2]. In order to minimize the power utilization for embedded system design [3] was proposed which quite succeeded in fulfilling the need. The gate input voltage had to be much more than the power supply for the SET for decent switching properties was proposed in [4] which eventually failed as it was practically unrealizable for building circuits.

3. Exploring Domino Logic Circuits

In order to overcome the occurrence of a hardware glitch because of dynamic logic, domino logic circuits were proposed. The general architectures of a domino logic stages is shown in Figure 2 and 3.

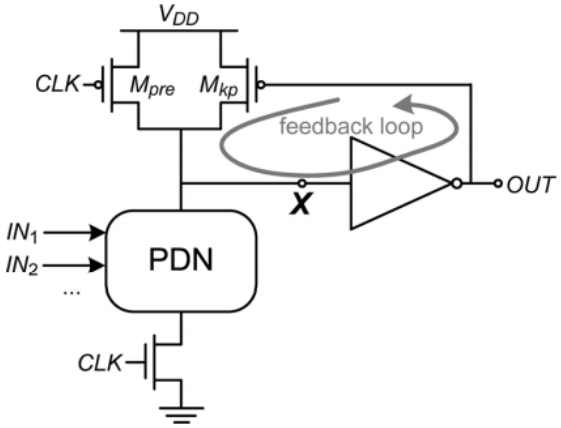

Figure 2. General architecture of Domino Logic

As seen in Figure 2, a Domino Logic contains a Pull Down Network(PDN) comprising only NMOS transistors. It contains a Precharge transistor and Evaluation transistor which works with every trigger of clock pulses. The architecture usually contains an inverter. Special enhancement to domino logic has introduced another transistor called keeper transistor. Figure 3 shows how number of Fan- in can affect the working of PDNs.

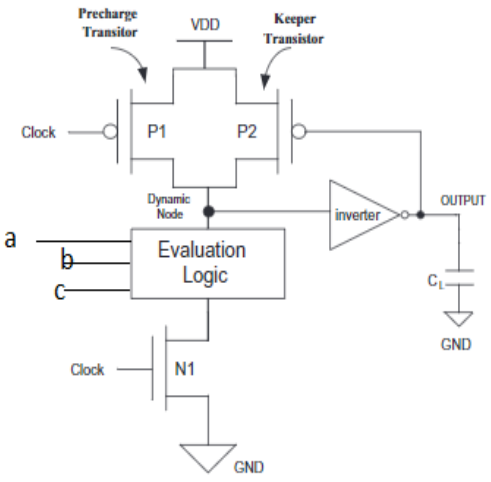

Figure 3. Architecture of Domino Logic with inputs

The inverter creates an output (with reference to Figure 2) as follows:$F\ (a, b, c) = \bar{F}$.This domino logic is basically non-inverting in nature because of a inverter at the exit part of

architecture. Domino logic works with clock values [12] in two phases.
Phase I: When clock $\phi = 0$, it initiates the pre changing phase where C_x pre changes to $V_x = V_{DD}$.
Phase II: When clock $\phi = 1$, it initiates the evaluation phase when the logic corresponding to the bank of nFETs are performed. Domino logic is always preferred in cascades. (i.e.,) output of 1st stage connected to input of next stage. But all stages are controlled by same clock signal ϕ.

Domino logic researches are going on from early 1990's. The various issues of domino logic circuits were discussed [5]. Later the variable threshold voltage keeper transistor was introduced to overcome the issues in noise margin [6].In this work, single electron transistors were used along with normal MOSFET's to overcome the issues associated with high power dissipation and more propagation delay of domino logic. Certain researches tried to incorporated single electron transistor with dynamic logic [7,13] where sets are used as pseudo transistors with great advantage that it is consistent in voltage levels and can be used for realizing hybrid circuits. A technique similar to our proposed work was elucidated in [9] but that used Fin FET Technology and analysed better noise performance and improve power delay product.

4. Proposed Domino Logic Architecture with SET in Pull-Down Network

Various CMOS logic architectures such as Inverter, NAND, NOR, OR, AND, EX-OR circuits were analysed. Their power, delay and area were found to be good enough for sustaining in the current scenario. But for future Nano-scale devices and technologies, we are in need of more precise and compact devices (deep sub-micron devices) [14,15] and therefore VLSI architectures. In this view, we have proposed using domino logic as an alternative to basic circuits as mentioned above. There is a twist to this switch over. We not only use normal MOSFET's, but also use SET's (Single Electron Transistor) in the architecture.

SET's are used only in the pull-down network of domino structures. Normal MOSFET's are used in the clock handling PMOS and NMOS part. This is because when clock is in pre-charge phase, the power dissipation will be higher than in the evaluation phase. To control power dissipation in pre-charge, MOSFET's are used. The architectures include for analysis are BUF, NAND2, NAND4, NOR2, NOR4, NOR8, and NOR16.

Even though SET's are used for bringing down the power consumption and area utilized. This proposed method also encounters the delay variation problem like normal domino logic. In order to overcome this delay variation, the loop and keeper transistors are utilized.

5. Keeper Transistor Modification Using SET

5.1 Analysis of Delay Variation

From [10], a small modification to our proposed method gave a good result even in the delay variations. Let us consider Figure 4 as a test circuitry for evaluation of delay variations. It is a well-known fact that there is always a trade-off between noise immunity and speed in domino logic circuit which basically rely on the keeper ratio (K) which is defined as the ration between saturation current of keeper transistor and overall pull down network. To overcome delay, K must be low than unity (preferably from 0.1 to 0.5). For this we need the PMOS of output in inverter four times wider than its NMOS.

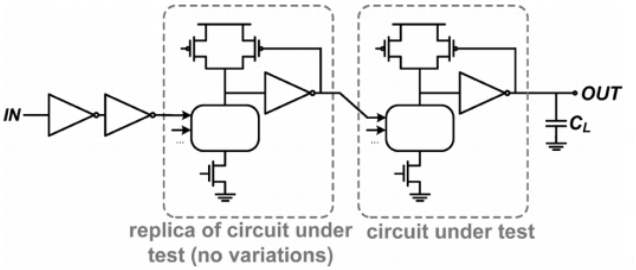

Figure 4. Circuit for evaluation of delay variations

In order to analyse delay variations, the above mentioned test circuit is treated with 200 runs of Monte Carlo simulations in 45nm CMOS spice tool. The Mean (μ), Standard Deviation (σ), Variability (σ/μ) are all noted for the delay. This test is done with load capacitance to kept at a minimum value by fixing the aspect ratio of inverter and PDN network as $(W/L)_{inv}$ is twice that of $(W/L)_{PDN}$. M_{kp} is sized to achieve keeper ratio K=0.1

5.2 Modifying Positive Feedback Loop to Reduce Delay Variations

A better architecture to split the keeper transistor and hence decrease its transconductance effect while keeping the same strength is shown in Figure 5.

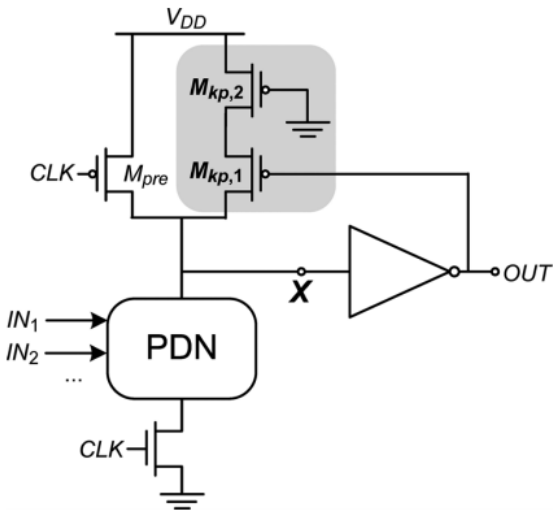

Figure 5. Split keeper transistors

(i.e) as per the methodology used in [10], the original keeper transistor is split into two M_{kp1} and M_{kp2} whose aspect ratios are accordingly

$$\left(\frac{L}{W}\right)_{kp1} + \left(\frac{L}{W}\right)_{kp2} = \left(\frac{L}{W}\right)_{kp}$$

Where kp→Keeper transistor; kp1 and kp2→ splitted values; (L/W) →inverse of Aspect Ratio to split kp equally, W→width of channel; L→Length of channel

To achieve this $W_{kp1} = W_{kp2} = W_{kp}$and $L_{kp1} + L_{kp2} = L_{kp}$ is followed. Even though the transistors are split, the resistance value will be maintained as given below:

$$R \cong [\mu p\ cox \left(\frac{W}{L}\right)_{kp2} (V_{DD} - |VtP|)]^{-1}$$

Where R→Dynamic Resistance; µp→mobility of PMOS; cox-→oxide capacitance; VDD→Supply voltage; Vtp-> threshold voltage of PMOS.

In our proposed system, the two split keeper transistors are also replaced with Single Electron Transistor (SET's). This modification brings down delay variations as well as improves the overall working performance of the domino logic circuits, with almost 80% decrease in power consumption and 63% decrease in speed.

6. Design Consideration, Simulation Results and Inferences

In the proposed work, the simulations for all the architectures are carried with the following specifications.

Pre-charge and Evaluation MOSFET Specification

The aspect ratios of precharge and Evaluation transistors are considered with the specification

$$(W/L)_{pre} = 1 \text{ and } (W/L)_{Eval} = 1$$

This can be achieved if

$$W_{pre} = W_{Eval} = 45nm \text{ and } L_{pre} = L_{Eval} = 45nm$$

6.1 Pull Down Network SET Specification

The aspect ratios of Pull Down Network transistors are considered with the specification

$$(W/L)_{PDN} \Rightarrow \text{series of } (W/L)_{SETS}$$

Which are having same aspect ratio as that of pre-charge and evaluation transistors but the channel insulation layer is very thin approximately 5 to 10nm.

6.2 Keeper Transistor Specification

As per the approach proposed in [10], for the reduced delay in domino logic, keeper transistor is split into two with following specification,

$$\left(\frac{L}{W}\right)_{kp1,SET} \text{ and } \left(\frac{L}{W}\right)_{kp2,SET}$$

$$W_{kp1} = W_{kp2} = 45nm$$

$$L_{kp1} + L_{kp2} = 45nm$$

$$L_{kp1} = L_{kp2} = 22.5nm$$

With these design consideration, the result obtained is 45nm CMOS Cadence SPICE tool with SET are discussed below. On an average of 10 buffer samples are considered for final values. In order to show the difference, CMOS logic is also included in the discussion of Table1.

Table 1 compares the Parameters considered for Area, Power, and Delay [11] constraints of a Buffer Architecture in CMOS logic, Traditional Domino with Keeper logic, and Domino with Split Keeper logic and proposed Domino with SET in PDN & Keeper logic (DSPK).

Table 1. Circuit Analysed: Buffer

Logic	Area (LUTS)	Power (mW)	Delay (ns)	Delay Variation (%)
CMOS	15	1.8	2.85	-
Traditional Domino with Keeper	13	1.632	5.19	8.86
Domino with Split Keeper	14	1.412	5.08	3.21
DSPK	**13**	**1.210**	**2.88**	**3.05**

Table 2 compares the Parameters considered for Area, Power, Delay constraints of a 2 input NAND Architecture in all four logic styles.

Table 2. Circuit Analysed: NAND2

Logic	Area (LUTS)	Power (mW)	Delay (ns)	Delay Variation (%)
CMOS	20	7.5	8.15	-
Traditional Domino with Keeper	18	6.99	10.53	10.34
Domino with Split Keeper	19	6.56	10.02	7.45
DSPK	**18**	**6.33**	**7.94**	**7.00**

Table 3 compares the Parameters considered for Area, Power, Delay constraints of a 4 input NAND Architecture in all four logic styles.

Table 3. Circuit Analysed: NAND4

Logic	Area (LUTS)	Power (mW)	Delay (ns)	Delay Variation (%)
CMOS	33	17.3	18.15	-
Traditional Domino with Keeper	28	16.69	12.73	12.76
Domino with Split Keeper	29	16.65	12.42	11.45
DSPK	**28**	**16.23**	**11.43**	**10.00**

Table 4 compares the Parameters considered for Area, Power, Delay constraints of a 2 input NOR Architecture in all four logic styles.

Table 4. Circuit Analysed: NOR2

Logic	Area (LUTS)	Power (mW)	Delay (ns)	Delay Variation (%)
CMOS	21	7.52	8.25	-
Traditional Domino with Keeper	19	6.97	10.89	10.50
Domino with Split Keeper	18	6.46	10.70	7.39
DSPK	**19**	**6.32**	**7.86**	**6.89**

Table 5 compares the Parameters considered for Area, Power, Delay constraints of a 4 input NOR Architecture in all four logic styles.

Table 5. Circuit Analysed: NOR4

Logic	Area (LUTS)	Power (mW)	Delay (ns)	Delay Variation (%)
CMOS	33	17.23	18.25	-
Traditional Domino with Keeper	28	16.95	12.37	13.86
Domino with Split Keeper	29	16.32	12.4	12.62
DSPK	**28**	**16.03**	**11.99**	**11.38**

Table 6 compares the Parameters considered for Area, Power, Delay constraints of an 8 input NOR Architecture in all four logic styles.

Table 6. Circuit Analysed: NOR8

Logic	Area (LUTS)	Power (mW)	Delay (ns)	Delay Variation (%)
CMOS	43	27.33	28.55	-
Traditional Domino with Keeper	38	26.00	22.73	23.86
Domino with Split Keeper	39	24.58	21.09	22.62
DSPK	37	24.00	21.20	11.00

Table 7 compares the Parameters considered for Area, Power, Delay constraints of a 16-input NOR Architecture in all four logic styles.

Table 7. Circuit Analysed: NOR16

Logic	Area (LUTS)	Power (mW)	Delay (ns)	Delay Variation (%)
CMOS	54	39.77	38.79	-
Traditional Domino with Keeper	47	36.25	32.45	28.55
Domino with Split Keeper	48	33.20	31.30	23.21
DSPK	**47**	**32.69**	**31.35**	**12.50**

From the above tables [1 to 7], it is inferred that when these structures are simulated and analysed in SPICE platforms like Cadence, the proposed system gives on an average an improvement of 80% improvement in power consumed and 63% improvement in speed. Thus 68% energy efficiency is obtained from the proposed architecture. This is achieved because of the effective usage of SETs in both PDN and Keeper transistors of Domino architectures. Also the delay variations are comparatively lesser than the conventional architectures of Domino logic. Moreover, the area utilized is also less making it prominent for Compact size applications especially Nano-electronics and other Nano applications.

7. Conclusion

The replacement of static CMOS logic in VLSI was never easier. Few steps have shown significant improvements in other logic styles as well but restricted to their applications. In this work also, the proposed hybrid architecture works with wonderful performance if used only for fundamental circuits. The effective replacement of MOSFET's with SET's both in pull down network and in keeper transistor have worked really well for improving power and delay variability performance in domino logic style. This will have its drawbacks for complex circuits as SET's will degrade noise immunity of domino. Hence, it is best suited for

simple basic gates which can find great application in Nano Technology like Nano electronics, Nano robotics. The future work of this paper will try to bring in SET's even more effectively into domino logic style. To conclude, this proposed work has brought 80% of power enhancement and 63% of delay improvement when compared with its predecessors.

Further this work can be continued by applying optimized aspect ratio values to SETs in PDN and keeper topology as a future work.

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