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Ensuring minimum duration of transient processes in switched voltage regulators with digital control

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Abstract

This paper describes a solution suggested to minimize the finite transient duration of a switched voltage regulator (SVR) for step changes in load current. SVR control laws aimed at minimizing the transient time are synthesized, and the microprocessor-based architecture and operating algorithms of the control system are designed. The prototype of the SVR digital control unit is implemented on the field-programmable gate array integrated circuit Cyclone III EP3C120F780 using the NIOS II soft-processor core. Embedded software is developed to calculate the control pulse duration for power switches in accordance with the synthesized control laws taking into account the feedback loop signal. A case study of the prototype shows that it provides the duration of transients caused by a load current step change, equal to 3-4 conversion periods at the frequency of 120 kHz. It confirms the suitability of the developed models, algorithms and control laws for ensuring the minimum transient duration.

Keywords: switching voltage regulator, SVR, control law, transient time, adjustable components of state variables, digital control loop, field-programmable gate array, FPGA.

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1. Introduction**

Electric and radio equipment requires stable power supply with low voltage deviations in stationary and dynamic operating modes. Requirements to power supply quality, including voltage stability, are regulated by such industry branch standards as National Aeronautics and Space Administration (NASA), European Space Agency (ESA) and European Cooperation for Space Standardization (ECSS) electrical power supply standards [1]. Voltage stabilization is carried out by switching voltage regulators (SVRs) [2, 3]. Power quality assurance is especially difficult for systems with multiple power sources and/or energy consumers [4]. To enhance voltage stability, efficient SVR control laws are being developed [5–7]. These control laws are usually implemented by a pulse width modulation (PWM)-based controller. Generally, PWM controllers are manufactured in the form of application-specific integrated circuits (ASICs) [8–10]. In addition to SVR control and voltage stability assurance, PWM controllers can perform a wide range of service functions, such as temperature control, circuit overload protection, etc. [11, 12].

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2. Problem statement

Requirements to power supply quality, including voltage stability, are becoming increasingly stringent. One of the most promising ways to meet them is to increase the performance of SVR, which allows us to reduce output voltage deviations for dynamic modes of operation. This is possible through developing new, more effective control laws. However, implementing an improved control algorithm with the use of existing series-produced PWM controllers is usually impossible due to mismatch of an internal controller structure with the new control law. For this purpose, small-scale integrated circuits and discrete components can be used, but this will decrease the reliability and increase the intrinsic power consumption of the SVR control unit, as well as its mass and size. Such negative changes in the characteristics of SVR are unacceptable.

The most appropriate and relevant to modern approaches should be considered the implementation of the SVR control unit based on a microprocessor platform with statically and dynamically reconfigurable architecture. Such a system can be developed as a “system-on-a-chip” on the base of ASIC, or partially or wholly field-programmable integrated circuit with an embedded microprocessor core. Reconfigurable microprocessor platforms allow performing both different algorithms of the SVR control and additional functions of SVR self-diagnostics, telemetry, etc. In addition, the proposed approach improves power supply system reliability in critical applications by including more than one SVR and allows implementing maximum power tracking algorithms for renewable energy sources, etc. [13, 14].

Of particular interest is a promising method for the synthesis of SVR control laws, described in [15], because it ensures high performance in output voltage stabilization. The proposed method includes:

- Representation of power circuits of SVR with PWM control in the mode of small deviations by a relevant pulse-amplitude model for describing adjustable components of the process.
- Synthesis of a control law using polynomial equations for designing pulse-amplitude modulation (PAM) systems [16].
- Implementation of the designed control law in a SVR taking PWM features into account.

The proposed method allows designing a control law that provides the minimum transient time in a step-down SVR. The schematic diagram of such a step-down SVR, or buck converter, is shown in Figure 1. It is based on the conventional SVR structure [17]. The difference is that the control unit (CU) is implemented usin a digital integrated circuit with an embedded microprocessor core.

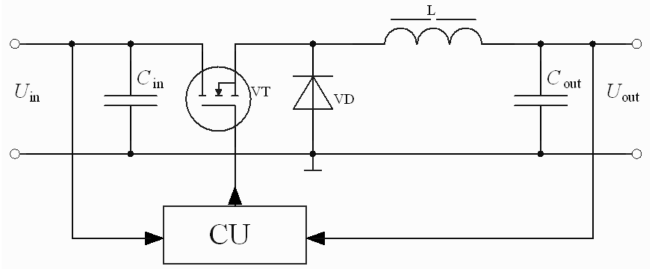

Figure 1. The schematic diagram of the buck converter

3. Control law synthesis

It is proposed to use the SVR control law synthesized on the base of described above method [15] as optimal in performance, and the SVR implementing this control law is to be called a high-performance SVR.

By adjustable components of the process, we mean deviations of variable parameters of the SVR from their values in the stationary mode, which are caused by an increase in the current pulse duration $t_{p.adj}$ relative to the stationary duration $t_{p.fix}$.

Let us consider selecting an adjustable component on the example of timing diagrams of the buck converter.

Figure 2 presents variations with time of the load current I_{load}, the inductor current I_L and its stationary $I_{L.fix}$ component, the output capacitor current I_C and its components: stationary $I_{C.fix}$ and adjustable $I_{C.adj}$, the adjustable component of the output capacitor voltage $U_{C.adj}$, the conversion period T, the pulse width t_p and its components: stationary $t_{p.fix}$ and adjustable $t_{p.adj}$, and sawtooth voltage of the PWM U_{glv}.

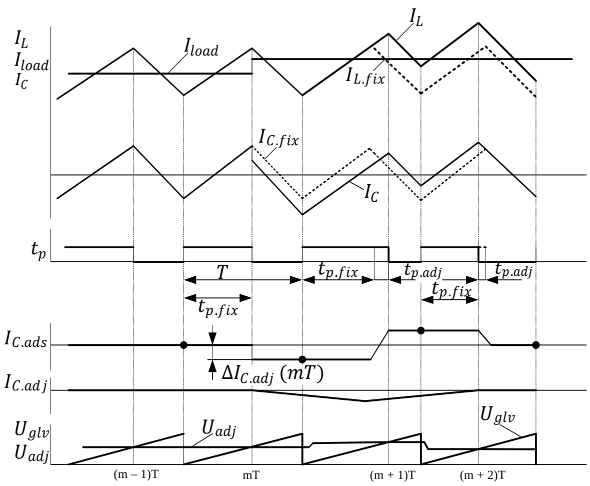

Figure 2. Timing diagrams of the buck converter

From the general SVR process with PAM control, a stationary process and a control process can be distinguished. The first corresponds to the constant (stationary) duration of control pulses $t_{p.fix}$ of the adjusting element. The second is due to increment of the control pulse duration t_p by the amount of $t_{p.adj}$ relative to the stationary duration $t_{p.fix}$. Useful information about the control process is only contained in adjustable components. In case of small deviations of the control pulse duration, the following condition is met: $t_{p.adj} << T$, where T is the commutation cycle duration.

In a system utilizing PWM, the adjustable component is given by voltage pulses $u_{L.p}(t)$ with duration $t_{p.adj}(t)$, that affect on the inductor from the adjusting element. To pass from PWM to PAM, they are replaced by δ-functions, which are equivalent in terms of the volt-second "area". It is acceptable in case of small deviations.

In [18], it is shown that the influence of the load conductance and the inductor internal resistance can be neglected for pulse amplitude SVR model in the case of use the optimal in performance control law. This allows us to represent a pulse-amplitude SVR model as connected an ideal pulse element and elements with transfer functions $1/pL$ and $1/pC$ in series (Figure 3).

The adjustable voltage component on the buck converter filter input represents bipolar pulses with amplitude $u_{L.adj}(t)$. The pulse width $t_{p.adj}(t)$ is equal to the deviation of the pulse width $t_p(t)$ from its stationary value $t_{p.fix}$. This determines the input signal of an ideal pulse element for the adjustable components of the pulse-amplitude modulation for the buck converter as:

$$s(t) = u_{L.\text{adj.a}}(t) t_{\text{p.adj}}(t).$$

Equation (1) corresponds to the proposed pulse amplitude buck converter model:

$$u_{L.\text{adj}}(t) = s(t)\delta^*(t), \tag{1}$$

where δ*(t) is a sequence of δ-functions with the period T, described by the following expression:

$$\delta^*(t) = \sum_{m=1}^{\infty} \delta(t - mT).$$

PWM-regulation for adjustable components in the field of lattice function transforms is determined by the equation:

$$U^*_{\text{out}}(p) = W^*_0(p) S^*(p), \tag{2}$$

where $U_{out}*(p)$ and $S*(p)$ are lattice function transforms for adjustable components the output voltage and the control signal respectively; $W_0*(p)$ is the discrete transfer function determined by the transfer function of the continuous part $Wcp(p)$ [15].

Only the adjustable components of the state variables carry useful information about the pulse-width control process. The constant component does not contain such information, and the pulsation of variable states is an information disturbance. This means that control laws for SVR should be synthesized on the basis of the expression (2) which describes the process of pulse-width control using adjustable components. Pulsations of state variables should be taken into account when implementing the control law.

Transformation of the pulse-width regulation to the amplitude-pulse regulation in the neighborhood of a stationary mode allows applying a well-developed mathematical apparatus of the PAM [15] for the analysis and synthesis of SVR with PWM control and to develop pulse-based control laws.

The block diagram of the designed pulse system is shown in Figure 3.

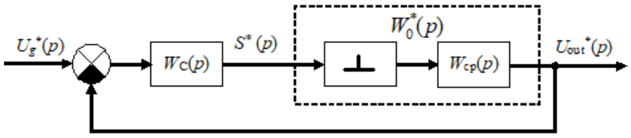

Figure 3. The block diagram of the synthesized pulse system

To synthesize the optimal in performance control law for the SVR, we use the third polynomial equation of synthesis [16]. This equation provides for synthesis of the discrete transfer function $W_C(p)$ for a feedforward compensator according to the condition of the minimum finite duration of processes in a closed system depending on external influences and in case of the deviation of the feedforward compensator parameters from calculated values. It ensures the practical feasibility of $W_C(p)$.

$$W^*_{C1}(p) = W^*_{C2}(p) = d_0 + d_1(1 - e^{-pT}), \tag{3}$$

where:

$$d_0 = d_1 = \frac{1}{T\omega_F^2},$$

$$\omega_F^2 = \frac{1}{LC},$$

L and C are the inductance and the capacitance of the output filter respectively.

4. Developed control methods of the switched voltage regulator

The control unit for a SVR with PWM control have been designed in accordance with the synthesized transfer function (3), taking specifics of pulse-width modulation into account. Two solutions are considered [15]. The first solution is control depending on instantaneous values of state variables. It suggests preliminary studying relationships between the stationary pulsation and the increment of duration of control pulse $t_{p.adj}(t)$, formed by the modulator, with considering this dependence thereafter (at the next step) [18]. A study of this solution proves achieving the transient time of 3–4 conversion periods, which is close to the theoretical limit of 2 periods for a second-order system with pulse-amplitude modulation [18]. At the same time, the study shows a significant static error of stabilization in the output SVR voltage. This is due to the fact that the gain of the feedback loop:

$$d_0 = d_1 = 1/(T\omega_F^2),$$

defined by expression (3), is obtained through parameters of the SVR power circuit. Therefore, its increase leads to decrease in performance [19]. In this case, astatism of the output voltage is provided by introducing a second integrating voltage feedback loop [20].

Thus, the input of the pulse-width modulator is the following:

$$u_{\text{int.M}}(t) = u_d(t) + u_{\text{int}}(t). \quad (4)$$

It is the sum of two signals. The first, $u_d(t)$, provides dynamical properties of the SVR. It is produced by the feedforward compensator according to equation (3). The second, $u_{int}(t)$, provides zero offset of the SVR output voltage. It is obtained by integrating the error signal $e(t)$ of the SVR output voltage:

$$u_{\text{int}}(t) = K_{\text{p}} \int_0^t e(t)dt + \text{U}_1, \quad (5)$$

where $e(t) = u_{out}(t) - U_0$, $u_{out}(t)$ is the SVR output voltage, U_0 is the reference voltage, $K_p << 4K_{opt} / (2rcC + T)$, where K_{opt} is the feedback gain factor that determines SVR dynamic properties, rc is the internal resistance of the output filter capacitor, C is the capacitance of the output filter capacitor.

The second solution is based on extracting adjustable components of SVR state variables at the beginning of a commutation cycle by special sample-and-hold elements. In the case of SVR implementation using microprocessor platform, this approach is preferable considering that it suggests the single-time sampling of signals at the beginning of each commutation cycle. In comparison, the first solution requires multiple analog-to-digital conversions of information signals. According to the second solution, the PWM input signal, which describes dynamic properties of the SVR, is described by the following equation:

$$U_d(mT) = U_d((m-1)T) + \Delta U_d(mT), \quad (6)$$

and its increment by the commutation cycle T is defined as follows:

$$\Delta U_d(mT) = \frac{LC}{U_{\text{in}} K_{\text{pwm}} \text{T}^2} \left[2\Delta U_{\text{c.adj}}(mT) - \Delta U_{\text{c.adj}}((m-1)T) \right], \quad (7)$$

where U_{in} is the SVR input voltage. The first difference of the SVR output voltage is determined as:

$$\Delta U_{\text{c.adj}}(mT) = U_{\text{c.adj}}(mT) - U_{\text{c.adj}}((m-1)T), \quad (8)$$

The PWM gain factor is described by the following equation:

$$K_{\text{pwm}} = \Delta t_{\text{t.adj}} / \Delta U_{\text{in.pwm}}(mT) = T/U_M, \quad (9)$$

where $\Delta t_{c.adj}$ is the increment of the control pulse duration, $\Delta U_{in.M}(mT)$ is the increment of the PVM input signal, U_M is the amplitude of the PWM sawtooth voltage [19].

Existing microprocessor technologies allow implementing the second approach to the SVR design [20], in correspondence with the optimal in performance control law and with the use of an integrating voltage feedback loop under control of the digital PWM controller.

5. Minimization of transient time

For the considered solution, minimization of the transient time is reduced to calculating the input signal of the PWM controller and producing through this signal the actual width-modulated pulse control signal for the SVR power switch, performed by a microprocessor unit. The PWM input signal is calculated using expression (10), which is obtained from equation (4) taking into account the discrete nature of signal processing:

$$U_{\text{in.M}}(mT) = U_d(mT) + U_{\text{int}}(mT). \quad (10)$$

The signal $U_d(mT)$ that determines SVR dynamic properties is defined by equations (6)–(8). The first difference of the adjustable component of the SVR output voltage, which is described by equation (8), can be described by the following expression:

$$\Delta U_{\text{C.adj}}(mT) = E(mT) - E((m-1)T), \quad (11)$$

where $E(mT)$ is the discrete value of the loop error signal on the SVR output voltage, which is determined taking into account (5) as follows:

$$E(mT) = U_{\text{out}}(mT) - U_0. \quad (12)$$

This replacement is acceptable because the SVR output voltage, presented as:

$$U_{\text{out}}(mT) = U_{\text{C.adj}}(mT) + U_{\text{fix}}(mT) + U_{\text{ripple}}(mT),$$

contains besides the adjustable component $U_{C.adj}(mT)$ the fixed component $U_{fix}(mT)$ and the ripple component $U_{ripple}(mT)$ that do not vary during a commutation cycle T.

Therefore, when calculating the first difference $U_{C.adj}(mT)$ using equation (11) and taking into account (12), the fixed component $U_{fix}(mT)$, the output voltage ripple $U_{ripple}(mT)$ and reference voltage U_0, biased in relation to each other by the commutation cycle T, are mutually subtracted. The signal $U_{int}(mT)$ providing astatism of the SVR, can be calculated by the expression:

$$U_{\text{int}}(mT) = K_{\text{p}} \sum_{k=1}^{m} E(kT), \qquad (13)$$

It is distinct from the expression (5) taking into account the replacement of integration by summation.

Information signals necessary for the SVR control, are the voltage at the input and output of the SVR. Their sampling is carried out at the time instants mT. Digital conversion and further calculations take the time interval $ts << T$. In the considered case, the SVR power switch performs modulating the leading edge of a control pulse. The delay in determining the control pulse width of the SVR power switch does not have a significant effect on the calculation result, because calculations are performed at the time interval when the power switch is turned off.

Figure 4 presents the block diagram of the signal processing sequence performed by the microprocessor control system.

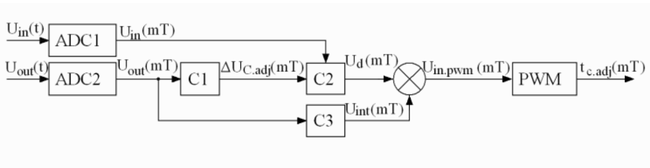

Figure 4. The block diagram of the signal processing sequence performed by the microprocessor control system

Analog-to-digital converters ADC1 and ADC2 provide sampling and analog to digital conversion of the SVR input voltage $u_{in}(t)$ and the output voltage $u_{out}(t)$ at time instants mT, i.e. define signals $U_{in}(mT)$ and $U_{out}(mT)$. Then, computing unit C1 calculates the first difference for the adjustable component of the output voltage $\Delta U_{C.adj}(mT)$ according to (11) in the vicinity of the time point mT. Thereafter, computing unit C2 defines the signal $U_d(mT)$, which is responsible for SVR dynamic properties. Computing unit C3 defines the signal $U_{int}(mT)$ which is responsible for astatism of the SVR output voltage. Then, the adder calculates $U_{in.pwm}(mT)$ by summing $U_d(mT)$ and $U_{int}(mT)$ according to (10). After that, the PVM controller defines the control pulse width tc.adj according to the equation $t_{c.adj} = K_M V_{in.pm}$ defined by (9). The obtained width will take effect during the next time period to time instants mT. The microprocessor control system synchronizes the falling edge of a control pulse with the time instant (m+1)T.

6. Implementation of designed control laws and control algorithms

To confirm the theoretical results obtained, a prototype of the buck converter with digital control is implemented. It is designed in accordance with the structure presented in Figure 1. The functional diagram of the buck converter is depicted in Figure 5.

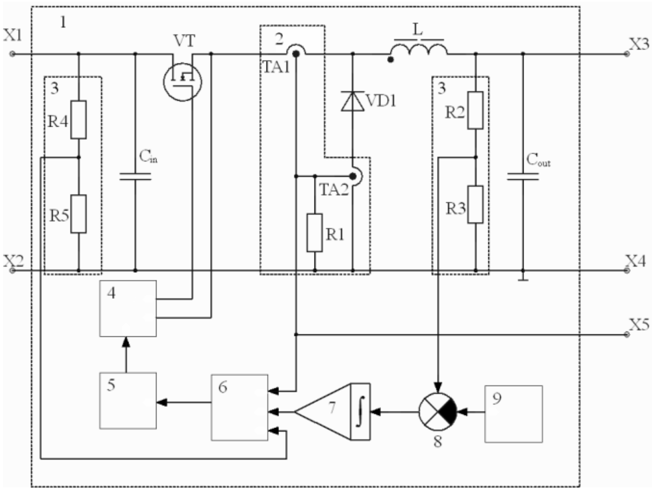

Figure 5. The functional diagram of the buck converter prototype

The power part (1) of the prototype includes:

- Power switch, made on the MOSFET transistor VT.
- Closing diode VD1.
- Input and output capacitors C_{in} and C_{out}.
- Induction L and inductor current sensor (2) (Figure 6), implemented on current transformers TA1 and TA2 and load resistor R1.

The control unit prototype includes:

- Voltage dividers (3) consisting of resistors R4, R5 and R1, R3.
- Driver (4) to control the transistor VT.
- Control automaton (5) on the base of Field Programmable Gate Array (FPGA) circuit Altera Cyclone III EP3C120F780 with integrated NIOS-II processor core.
- Analog-to-digital converter (6) based on max1308.
- Analog integrator (7) and adder (8), implemented on an operational amplifier.
- Reference voltage source (9).

The schematic diagram of current transformers TA1 and TA2 with a demagnetizing resistor R is shown in Figure 6.

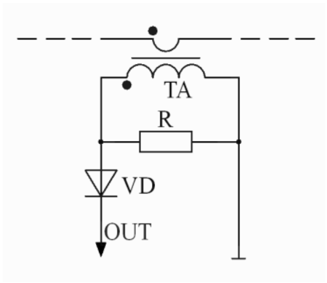

Figure 6. Inductor current sensor

The buck converter prototype has the following main characteristics:

- the buck converter output voltage u_{out} = 28 V,
- the input voltage u_{out} varies from 40 V to 110 V,
- the conversion frequency f_c = 120 kHz,
- the capacitance of the input C_{in} and output C_{out} filter capacitors is 1000 μF ;
- the inductance L = 180μH at the 1.5A inductor current and L = 120 μH at the 4 A inductor current.

The prototype is designed to determine dynamic characteristics close to the maximum possible, in combination with the output voltage astatism in static operating modes.

The control unit implements the algorithm of generating control signals for the buck converter power switch at the microprogram level. The algorithm is presented in Figure 7. In calculations, the average inductance is assumed 150 μH.

Embedded software for the microprocessor control unit has been developed. At the first stage, the software time delay of the first sample is introduced. This is performed in order to finish transients of digital and analog modules and reach operating mode of power supply electronic components. During this delay, the variables are initialized, the control subsystems are set, the system constants are defined, such as the initial value of the control signal pulse duration ($t_{c.st}$), the pulse width, the modulation period of the signal, the value of the reference voltage U_0, etc. Hereinafter, time interval lines are implemented at the hardware-software level using programmable timer-counters.

At the end of the software delay, a sync signal is received from the main timer. After receiving the sync signal, the signal for controlling power switches is generated. In the first program cycle, the width of the power switch control pulse $t_{c.adj}$ (MT) is set by the initial value tc.st, which is necessary for starting the buck converter. Then, input signals are synchronously converted by ADC 1 and 2 (Figure 4) into the digital format of the values $U_{in}(mT)$ and $U_{out}(mT)$ respectively. ADCs operate in parallel; the beginning of the conversion is synchronized. The ADCs perform conversion during a small offset interval τ <0.25T, i.e. during the first quarter of the period. There may be some temporary mismatch in the completion of the conversion steps. However, difference of digitization time is insignificant, of the order of 10^{-12} seconds. This does not affect results in the calculation time intervals and is synchronized when receiving data from the ADC by the microprocessor unit in the direct memory access mode.

At the end of the measurements, correction values are calculated. Next, the duration of power switch control pulse is calculated for the next program cycle, corresponding to the time instant $mT + 1$. The calculation is performed in accordance with the formula (10) by the expression:

$$t_{c.adj}(mT) = K_{pwm}U_{in.pwm}(mT)$$

In more detail, the algorithm of the developed embedded software is shown in Figure 7.

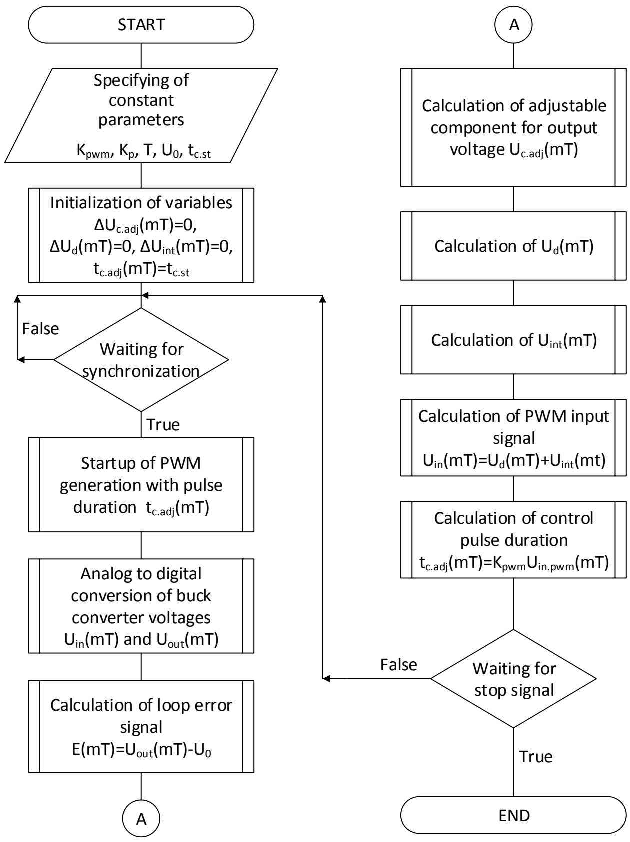

Figure 7. The algorithm of the embedded software for buck converter controller

7. Experimental results

To study buck converter prototype, a test facility was developed. The functional diagram of the installation is depicted in Figure 8.

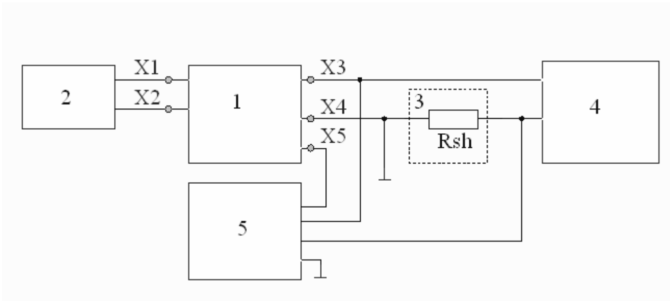

Figure 8. The functional diagram of the test facility

The test facility includes: buck converter prototype (1), power supply with adjustable supply voltage range from 40 V to 110 V (2), current sensor in the form of a resistive *Rsh* shunt with a resistance of 0.2 Ohm (3), a load unit consisting from constantly connected and periodically switched resistors (4) and a four-channel oscilloscope (5).

The results of studying the buck converter prototype are shown in Figures 9–11.

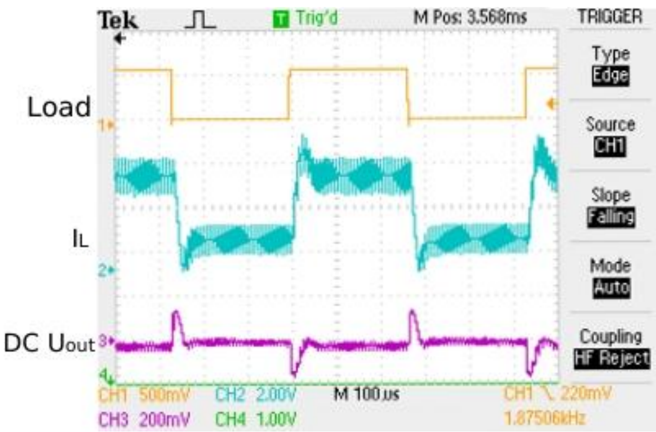

Figure 9. Step change in output current

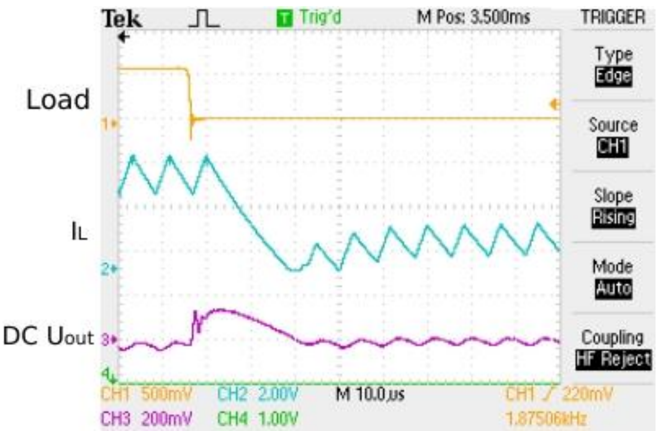

Figure 10. Step decrease in output current

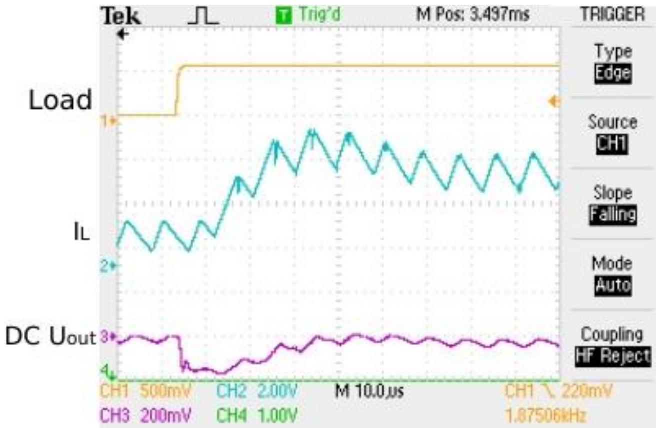

Figure 11. Step increase in output current

In all figures the first signal from the top (Load) represents the load current change in 2.5 A/div scale, the second signal (I_L) represents the inductor current in 2 A/div scale, the third signal (DC Uout) is the adjustable component of the buck converter output voltage in 0.2 V/div scale. The fixed component of a load current is shown in the figure partly. The timescale is 100 µs/div. Processes that comprise two commutation cycles of the step load current change are shown in Figure 9. The constant component of the load current is 1.4 A, and the step load current increment is 2.8 A. Figure 3 proves out that the control process meets the zero offset requirements because the output voltage returns to its initial value after finishing the transient process. Further tests confirm the absence of the output voltage offset even if the buck converter input voltage varies in the range mentioned above. Figure 10 and Figure 11 show step load current decrease and step load current increase processes on a large scale respectively. The transient time is approximately 5–6 commutation cycles for the step load current decrease process (fig. 6) that is close to the minimum possible transient time. The transient time is approximately 6–8 commutation cycles for the step load current increase process (figure 7). Increase in the transient time relative to its minimum value is explained by the determined limitation of the maximum control pulse width at 0.75T. The reason of limiting the pulse width is the need for an additional time interval for demagnetization of the inductor current sensor based on the transformer, analog-to-digital converting informational signals and calculating the width of the buck converter control pulse.

8. Conclusion

In this paper, a solution is proposed for minimizing finite duration of transients in a step-down switched voltage regulator (buck converter) with step changes of the load current. The solution implements a method of control law synthesis, which, according to preliminary studies, should provide high performance in stabilizing the SVR output voltage. The proposed method uses the representation of the

SVR power circuits in the mode of small input voltage deviations by a relevant pulse-amplitude model for describing adjustable components of the process. The synthesis of SVR control laws is performed using polynomial equations for designing PAM control and implementation of the designed control law in the SVR considering PWM features. This method allows designing a control law that provides the minimum transient time in a step-down switched voltage regulator. A microprocessor platform with statically and dynamically reconfigurable architecture is suggested as the most relevant hardware platform for the SVR control unit. The prototype of the buck converter with digital control unit is implemented using a FPGA circuit with an integrated processor core.

Experimental studying the prototype proves the efficiency of the proposed method. In case of a step change of the load current, the described solution provides the minimum finite duration of transients equal to 5-6 conversion periods, approaching the lowest theoretically possible limit. The experiments show that single sampling and analog-to-digital conversion of input signals, and calculating correction values of the control pulse during a commutation cycle T, releases significant time resources of the microprocessor control unit. The released time resource can be utilized to diagnose the buck converter or to distribute the load current between several buck converters operating in parallel for the common load and other maintenance functions, which is an additional advantage of the proposed buck converter control method. The use of switching power supply with digital control unit implemented by means of high-performance microprocessor systems provides significant strategic advantages over analog systems.

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